Industrial SATAⅢ mSATA

Solid State Drive E-Series

DRAM LESS

(SanDisk Bics4 3D-TLC)

データシート

株式会社アドテック

Revision History

Revision	Description	Date
V1.0	New release	May 2022

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1．Product Description

1.1. Product Overview

ADTEC SATAIII mSATA SSD is the storage device based on NAND flash memory technology. This product complies with JEDEC standard form factor and Serial ATA standard interface and suitable for data storage media and code storage device for embedded system and boot disk. By using mSATA, it is possible to operate good performance for the systems, which have SATA interface. With small form factor, the applicable appliance can add or install SATA storage device on its Mother Board or Complete set.

1.2. Product Features

- High performance and reliability.
- Small form factor refers to the MO-300 specification which established by JEDEC.
- Support AEC 256bit encryption.
- Build-in Global Wear-leveling and Hardware Advanced LDPC ECC engine.
    - Correct capability up to 250 bits per 2Kbytes.
    - Optional Advanced RAID/XOR engine for higher error correction capability.
- Compliant with SATA III 6.0Gbps (backward compatible to 3 Gb/s 1.5 G/s).
- Operating as Boot Disk.
- Support S. M. A. R. T., DEVLP mode, Security & Trim command.
- Noiseless and stable installation to system.
- Silent, low-power operation. Resistant to shock and vibration.
- Memory Capacities
  3D-TLC: 60GB / 120GB / 240GB / 480GB / 960GB

- Automatic sleep and wake-up mechanism to save power.
- Compliant with Serial ATA Revision 3.1 / ATA-8 specification.
- Supports Bad Block Management.
- Fully Compliant with RoHS directive.
- CE and FCC Compatibility.

1.3. Specifications

Interface	SATAIII 6Gb/s compatible
NAND Flash Type	3D-TLC
Controller	ET6311B
Form Factor	MO-300
Connector Type	mSATA (52 pin)
Capacity	3D-TLC: 60GB / 120GB / 240GB / 480GB / 960GB
Power Consumption (Max)	<1025mW
Operating Temperature	0°C ~ +70°C
Storage Temperature	-40°C ~ +85°C
Humidity	0°C~55°C /10~95%, non-condensing
TRIM	Yes
S.M.A.R.T (Health Monitor)	Yes
Vibration (Operating)	20GPeak, 10 ~ 2000Hz
Shock	1500G,0.5ms
Dimension (L x W x H)	50.95 x 30.00 x 3.90mm

Table 1: mSATA SSD Specifications

1.4. Performance

Type	Capacity	Sequential (QD32)		Sequential		Random (4KB)		Random (4KB QD32)	
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)	Read (IOPS)	Write (IOPS)
3D-TLC	60GB	536.2	200.8	416.5	203.2	7066	30362	25856	42650
	120GB	550.6	370.9	491.0	364.7	6963	18688	38298	34586
	240GB	541.3	423.3	471.2	381.7	7066	30566	64896	51994
	480GB	545.7	429.3	409.8	381.5	7706	26931	65152	51686
	960GB	529.4	485.6	450.1	417.8	8397	22963	80000	71680

*Performance may vary based on SSD capacity, hardware test platform, test software, operating system and other system variables.

Table 2: mSATA SSD Performance

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1.5. TBW (Tera Bytes Written)

Capacity	TBW
60GB	40TB
120GB	80TB
240GB	160TB
480GB	320TB
960GB	640TB

*All documented endurance test results are obtained in compliance with JESD218 Standards.

See www.jedec.org for detailed definitions of JESD218 Standards.

Table 3: mSATA SSD TBW

1.6. System Requirement

The Host system which is connected to mSATA SSD should meet system requirements at minimum.

1.6.1. Power Requirement

Item	Symbol	Rating	Unit
Input voltage	VIN	+3.3V DC ± 5% 1000mA (max.)	V

Table 4: mSATA SSD Power Requirement

1.6.2. Operating System
- Windows family.
- Linux family.
- DOS or embedded system.

1.6.3. Interface
- SATA Interface.

2．Detailed Specification
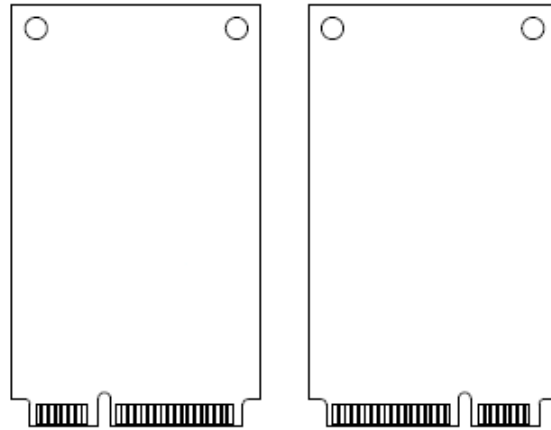
2.1. Physical Specifications
2.1.1. Overlook

Figure 1: mSATA SSD Overlook Diagram

2.1.2. Dimension
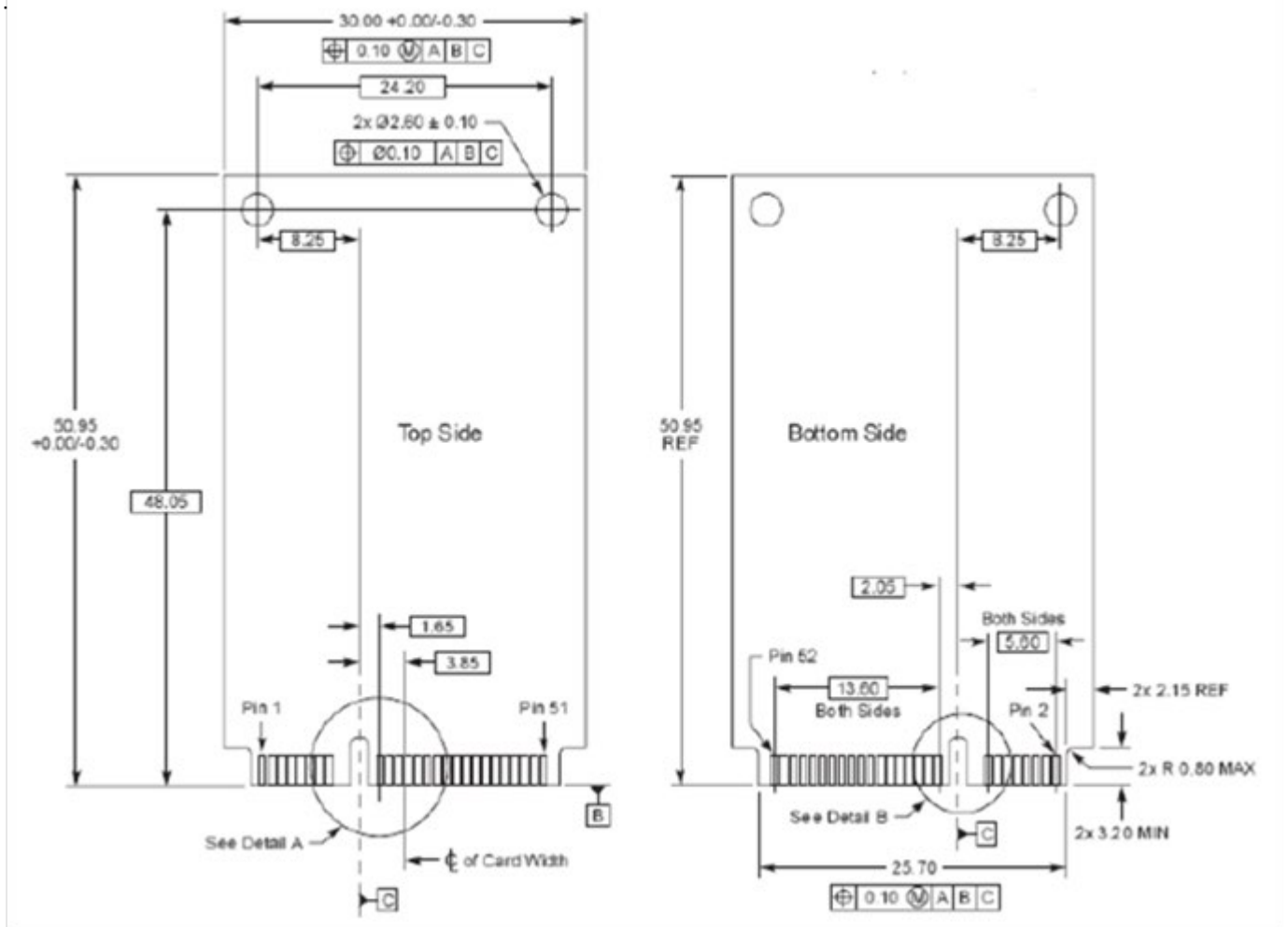
Figure 2: mSATA SSD Module Dimensions

Parameter	Specifications
Width	30.00mm ± 0.30mm
Length	50.95mm ± 0.30mm
Height	3.90mm ± 0.30mm

Table 5: mSATA SSD Module Physical Dimension

2.2. Electronic Specifications

2.2.1. Product Definition

mSATA SSD Module is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through Serial ATA Standard Interface to Host Systems.

Figure 3: mSATA SSD Block Diagram

2.2.2. Pin Signal Assignment

The signals assigned for Serial ATA applications are described in Table 6.

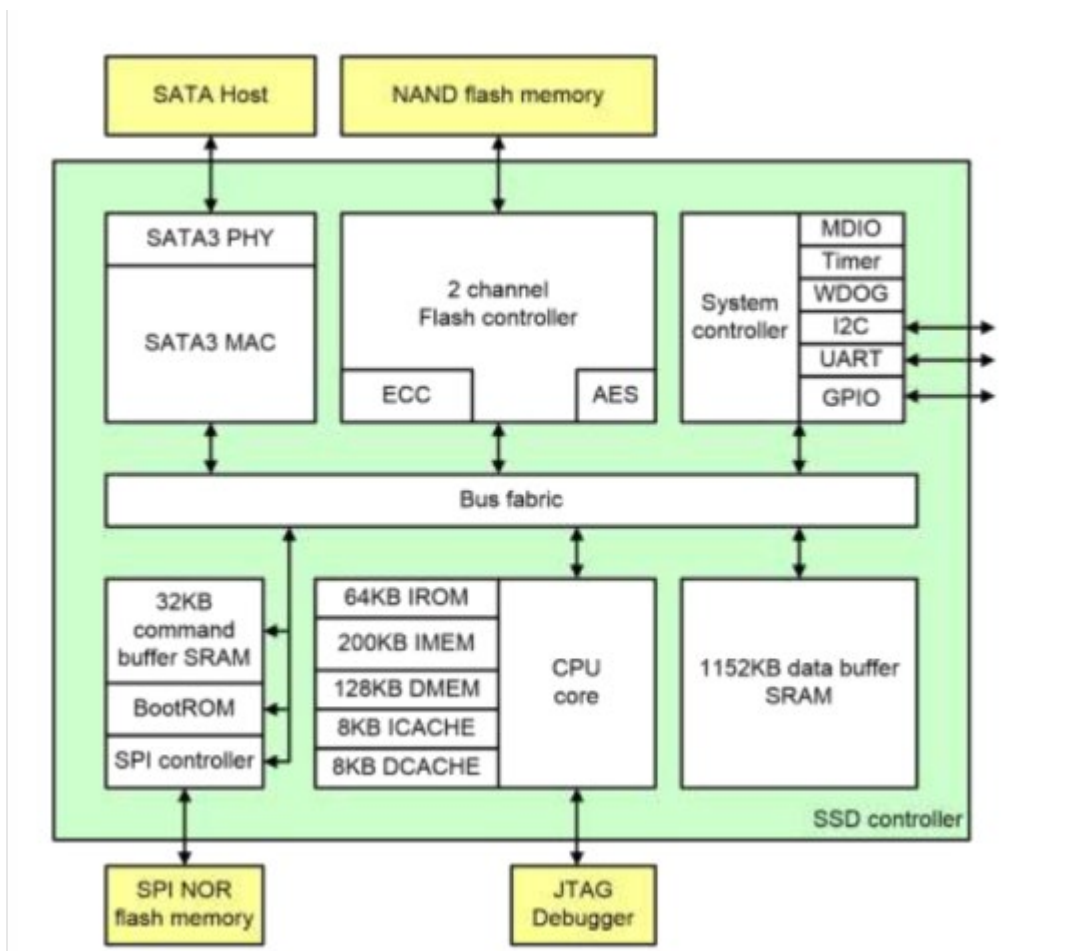| Pin definition	Pin No.
GND	4,9,15,18,21,26,27,29,34,35,37,40,43,50
3V3 power +in	2,24,39,41,52
SATA Txn	25
SATA Txp	23
SATA Rxn	31
SATA Rxp	33
Presence Detection	51
DA/DSS	49

Signal Name	Pin #	Pin #	Signal Name
Presence Detection	51	52	+3.3V
DA/DSS	49	50	GND
NC	47	48	NC
NC	45	46	NC
GND	43	44	NC
+3.3V	41	42	NC
+3.3V	39	40	GND
GND	37	38	NC
GND	35	36	NC
+A – RX-	33	34	GND
-A – RX-	31	32	NC
GND	29	30	NC
GND	27	28	NC
-B – TX-	25	26	GND
+B – TX-	23	24	+3.3V
GND	21	22	NC
NC	19	20	NC
NC	17	18	GND
GND	15	16	NC
NC	13	14	NC
NC	11	12	NC
GND	9	10	NC
NC	7	8	NC
NC	5	6	NC
NC	3	4	GND
NC	1	2	+3.3V

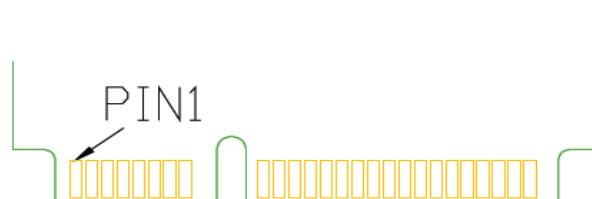Table 6: mSATA SSD connector pin definition

Figure 4: mSATA SSD Connector Pin Assignment

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2.3. Support ATA Commands

ATA Command Set summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Command	Code	Protocol
General Feature Set		
Execute Drive Diagnostic	90h	Device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

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Command	Code	Protocol
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

Table 7: ATA Command List

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2.4. SMART Attributes

The following table defines the vender specific data in bytes 2 to 361 of the 512-byte SMART data.

Attribute ID	Raw Attribute Value						Attribute Name
0x05	LSB	MSB	0	0	0	0	Later Bad Block count
0x09	LSB			MSB	0	0	Power-On Hours
0x0C	LSB	MSB	0	0	0	0	Power cycle count
0xA0	LSB	MSB	0	0	0	0	Uncorrectable sector count when read/write
0xA1	MSB	0	0	0	0	0	Valid spare block count
0xA3	LSB			MSB	0	0	Initial bad block count
0xA4	LSB			MSB	0	0	Total erase count
0xA5	LSB	MSB	0	0	0	0	Maximum P/E cycle
0xA6	LSB			MSB	0	0	Total Bad Block count
0xA7	LSB			MSB	0	0	Average erase count
0xAF	LSB			MSB	0	0	Reallocation event count
0xC0	LSB	MSB	0	0	0	0	Abnormal Power Cycle Count
0xC2	MSB	0	0	0	0	0	Controller temperature
0xC4	LSB			MSB	0	0	ECC fail count
0xC7	LSB			MSB	0	0	Ultra DMA CRC error count
0xCE	LSB	MSB	0	0	0	0	Minimum erase count
0xCF	LSB	MSB	0	0	0	0	Maximum erase count
0xF1	LSB			MSB	0	0	Write lifetime (GB)
0xF2	LSB			MSB	0	0	Read lifetime (GB)

Table 8: SMART Attributes

2.5. Shock & Vibration

Reliability	Test Conditions	Reference Standards
Vibration	10Hz to 2KHz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500G, 3 axes	IEC 68-2-27

Table 9: Shock/Vibration Testing for 2.5" SATA SSD

2.6. Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a hardware LDPC ECC engine that can correct 250 bits per 2K bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.7. Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the erase cycle limit or write endurance limit and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

mSATA uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

2.8. Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped or may generate during the lifetime of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management and replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit. After the reserved block less than 10 of each channel, the SSD will be locked, and cannot be read and written anymore. Host can send a vendor ATA command to unlock the SSD for backup data or system from SSD.

2.9. Mean Time between Failures (MTBF)

Failure Rate: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.

Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Product	Condition	MTBF (Hours)
mSATA SSD	Telcordia SR-332 GB, 25°C	>2,000,000

Table 9: mSATA SSD MTBF

2.10. Endurance

■ Flash Endurance: 3D-TLC: 3,000 P/E Cycle
■ Wear-Leveling Algorithm: Support.
■ Bad Blocks Management: Support.
■ Error Correct Code: Support.

2.11.　Transfer Mode

■ mSATA SSD support following transfer mode:
  ● Serial ATA I 1.5Gbps
  ● Serial ATA II 3.0Gbps
  ● Serial ATA III 6.0Gbps

3．Installation Requirements

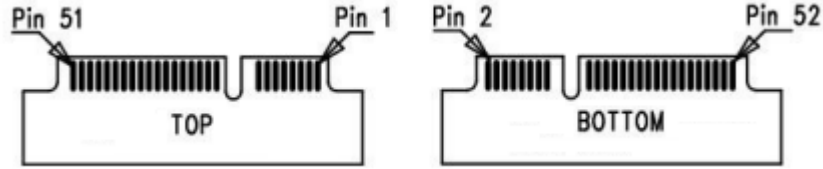## 3.1. mSATA Pin Directions

Figure 5: Signal Segment and Power Segment

3.2. Electrical Connections for mSATA

A Serial ATA device may be either directly connected to a host or connected to a host through an adaptor card. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

3.3. Device Drive

No additional device drives are required. The mSATA can be configured as a boot device.

4. Ordering Information

P/N	Capacity	Remark
ADOSS3060G3DCENES	60GB	SanDisk Bics4 3D-TLC Normal Temp
ADOSS3120G3DCENES	120GB	
ADOSS3240G3DCENES	240GB	
ADOSS3480G3DCENES	480GB	
ADOSS3960G3DCENES	960GB	

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