Industrial PCIe Gen3 x4 M.2(2280)

Solid State Drive E-Series

DRAM LESS

(SanDisk Bics4 3D-TLC)

データシート

株式会社アドテック

Revision History

Revision	Description	Date
V1.0	New release	May 2022

Table of Contents

1. Product Description

1.1. Product Overview

'ADTEC PCIe Gen3 x4 M.2(2280)' is the storage device based on NAND flash memory technology.
This product complies with JEDEC standard form factor and PCIe/NVMe standard interface and suitable for data storage media and code storage device for embedded system and boot disk.
By using M.2 SSD, it is possible to operate good performance for the systems, which have M.2 interface. With small form factor, the applicable appliance can add or install PCIe storage device on its Mother Board or Complete set.

1.2. Product Features

- High performance and reliability.
- Small form factor with PCIe/NVMe Standard Interface connector (M.2).
- Build-in Global Wear-leveling and Hardware Advanced LDPC ECC engine.
  - Correct capability up to 350 bits per 2Kbytes.
- Compliant with PCIe Gen3 up to 4-lanes support.
- Memory Capacities
  - 3D-TLC: 120GB / 240GB / 480GB / 960GB
- Data Security
  - Build-In AES 256 encryption.
  - TCG Opal 2.0 Compliant.
  - Support SHA256
- Support AHCI as well as NVMe.
- Support S. M. A. R. T. function.
- Support Intel CPPM total set.
- Support SRiS for cable less.
- Sudden power-fails management.
- Noiseless and stable installation to system.
- Silent, low-power operation. Resistant to shock and vibration.
- Automatic sleep and wake-up mechanism to save power.
- Operating as Boot Disk.
- Supports Bad Block Management.
- Fully Compliant with RoHS directive.
- CE and FCC Compatibility.

1.3. Specifications

Interface	PCIe Gen3 x4 compatible
NAND Flash Type	3D-TLC
Controller	ET7315
Form Factor	M.2 (NGFF) 2280
Connector Type	NVMe (75 pin)
Capacity	3D-TLC: 120GB / 240GB / 480GB / 960GB
Performance (Max)	Read: 3200MB/s, Write: 2500MB/s
Power Consumption (Max)	< 7W
Operating Temperature	0°C ~ +70°C
Storage Temperature	-40°C ~ +85°C
Humidity	0°C~55°C /95% RH
S.M.A.R.T (Health Monitor)	Yes
Dimension (L x W x H)	80 x 22 x 2.2mm

Table 1: M.2 PCIe SSD Specifications

1.4. Performance

Type	Capacity	Sequential (QD32)		Sequential (512KB)		Random (4KB)		Random (4KB QD32)	
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)	Read (IOPS)	Write (IOPS)
3D-TLC	120GB	1870.7	412.2	338.2	383.0	14546	50944	86272	97792
	240GB	1793.4	659.3	507.4	415.9	12872	40218	93030	93261
	480GB	1716.1	1318.5	1014.8	831.8	11195	29466	99789	88730
	960GB	1697.5	1540.0	809.0	848.7	10112	32998	104269	89779

*Performance may vary based on SSD capacity, hardware test platform, test software, operating system and other system variables.

Table 2: M.2 PCIe SSD Performance

1.5. TBW (Tera Bytes Written)

Capacity	TBW
120GB	80TB
240GB	160TB
480GB	320TB
960GB	640TB

Table 3: M.2 PCIe SSD TBW

1.6. System Requirement

The Host system which is connected to M.2 PCIe SSD should meet system requirements at minimum.

1.6.1. Power Requirement

Item	Symbol	Rating	Unit
Input voltage	VIN	+3.3V DC ± 5% 1000mA (max.)	V

Table 4: M.2 PCIe SSD Power Requirement

1.6.2. Operating System

- Windows family.
- Linux family.
- DOS or embedded system.

2. Detailed Specification

2.1. Physical Specifications

2.1.1. Overlook

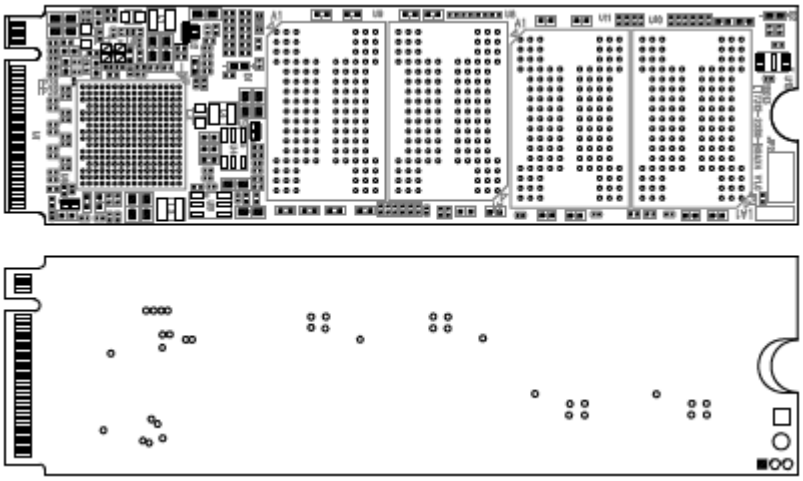

Figure 1: M.2 PCIe SSD Overlook Diagram

2.1.2. Dimension

The Dimensions of M.2 PCIe SSD are illustrated in Figure 2 and described in Table 6.

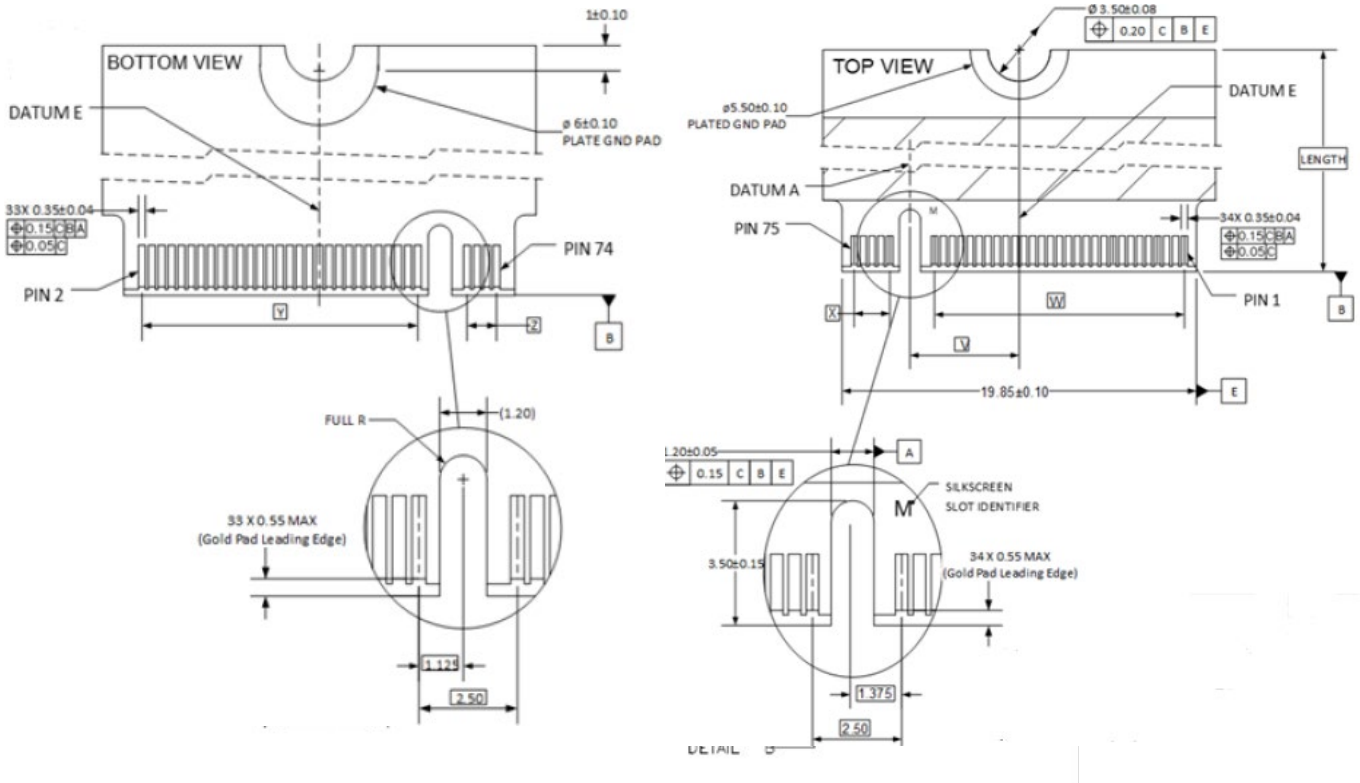

Figure 2: M.2 PCIe SSD Module Dimensions

Parameter	Specifications
Width	22.0mm ± 0.15mm
Length	80.0mm ± 0.15mm
Thickness	2.2mm ± 0.1mm

Table 6: M.2 PCIe SSD Module Physical Dimension

2.2. Electronic Specifications

2.2.1. Product Definition

M.2 PCIe SSD is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through PCIe/NVMe Standard Interface to Host Systems.

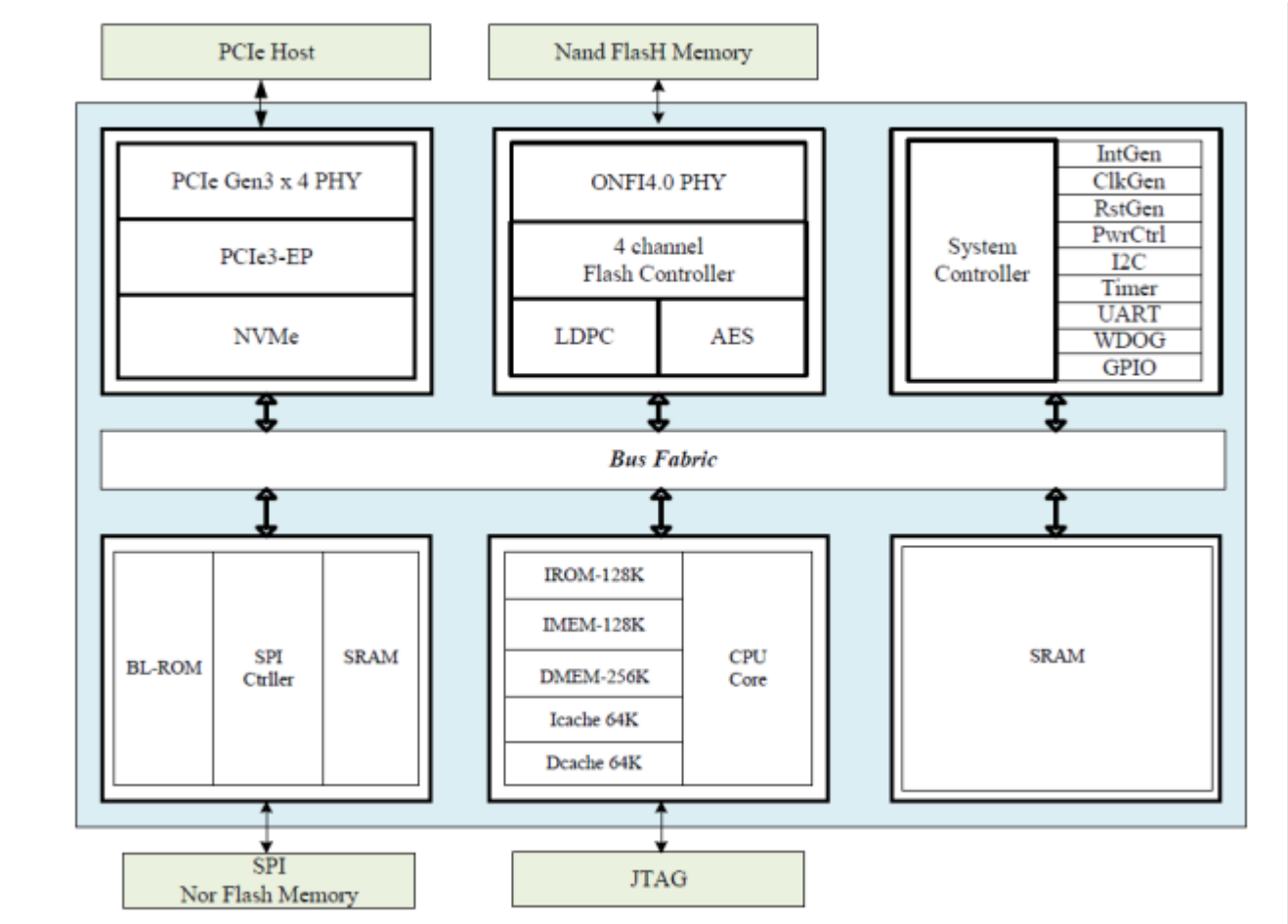

Figure 3: M.2 PCIe SSD Block Diagram

2.2.2. Pin Signal Assignment

The signals assigned for PCIe/NVMe applications are described in Table 7.

PIN	Function	Description	PIN	Function	Description
74	+3.3V	3.3V power	75	GND	Ground
72	+3.3V	3.3V power	73	GND	Ground
70	+3.3V	3.3V power	71	GND	Ground
68		DNC	69		DNC
		Connector Key	67		DNC
		Connector Key			Connector Key
		Connector Key			Connector Key
		Connector Key			Connector Key
58		DNC			Connector Key
56		DNC	57	GND	Ground
54		DNC	55	REFCLKp	Reference clock p
52	CLKREQ#	Clock request	53	REFCLKn	Reference clock n
50	PERST#	PCIe Fundamental Reset	51	GND	Ground
48		DNC	49	PERp0	PCIe RX Lane 0 p
46		DNC	47	PERn0	PCIe RX Lane 0 n
44	ALERT#		45	GND	Ground
42	SMB_DATA		43	PETp0	PCIe TX Lane 0 p
40	AMB_CLK		41	PETn0	PCIe TX Lane 0 n
38		DNC	39	GND	Ground
36		DNC	37	PERp1	PCIe RX Lane 1 p
34		DNC	35	PERn1	PCIe RX Lane 1 n
32		DNC	33	GND	Ground
30		DNC	31	PETp1	PCIe TX Lane 1 p
28		DNC	29	PETn1	PCIe TX Lane 1 n
26		DNC	27	GND	Ground
24		DNC	25	PERp2	PCIe RX Lane 2 p
22		DNC	23	PERn2	PCIe RX Lane 2 n
20		DNC	21	GND	Ground
18	+3.3V	3.3V power	19	PETp2	PCIe TX Lane 2 p
16	+3.3V	3.3V power	17	PETn2	PCIe TX Lane 2 n
14	+3.3V	3.3V power	15	GND	Ground
12	+3.3V	3.3V power	13	PERp3	PCIe RX Lane 3 p
10	LED1#	Status indicator for system LED	11	PERn3	PCIe RX Lane 3 n
8		DNC	9	GND	Ground
6		DNC	7	PETp3	PCIe TX Lane 3 p
4	+3.3V	3.3V power	5	PETn3	PCIe TX Lane 3 n
2	+3.3V	3.3V power	3	GND	Ground
			1	GND	Ground

Table 7: M.2 PCIe SSD connector pin definition

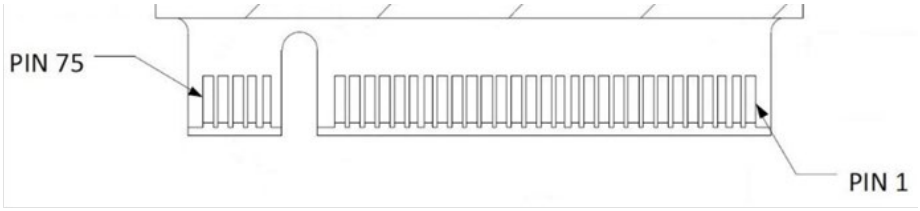

Figure 4: M.2 PCIe SSD Connector Pin Assignment

2.3. Support Commands

Command Set summaries the command set with the paragraphs that follow describing the individual commands and the task file for each.

Command	Code	Protocol
General Feature Set		
Execute Drive Diagnostic	90h	Device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

Command	Code	Protocol
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

Table 8: Command List

2.4. Shock & Vibration

Reliability	Test Conditions	Reference Standards
Vibration	10Hz to 2KHz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500G, 3 axes	IEC 68-2-27

Table 9: Shock/Vibration Testing for M.2 PCIe SSD

2.5. Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a hardware LDPC ECC engine that can correct 350 bits per 2K bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.6. Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the erase cycle limit or write endurance limit and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

M.2 uses a ‘advanced wear-leveling’ algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

2.7. Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed.

The Bad Blocks may be presented while the SSD is shipped or may generate during the lifetime of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management and replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit. After the reserved block less than 10 of each channel, the SSD will be locked, and cannot be read and written anymore. Host can send a vendor ATA command to unlock the SSD for backup data or system from SSD.

2.8. Mean Time between Failures (MTBF)

Failure Rate: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.

Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Product	Condition	MTBF (Hours)
M.2 PCIe SSD	Telcordia SR-332 GB, 25°C	>2,000,000

Table 10: M.2 PCIe SSD MTBF

2.9. Endurance

- Flash Endurance: 3D-TLC: 3,000 P/E Cycle
- Wear-Leveling Algorithm: Support.
- Bad Blocks Management: Support.
- Error Correct Code: Support.

2.10. Transfer Mode

- M.2 PCIe SSD support following transfer mode:
  - PCI-Express Gen-3 x4 Lane

3. Installation Requirements

3.1. M.2 Pin Directions

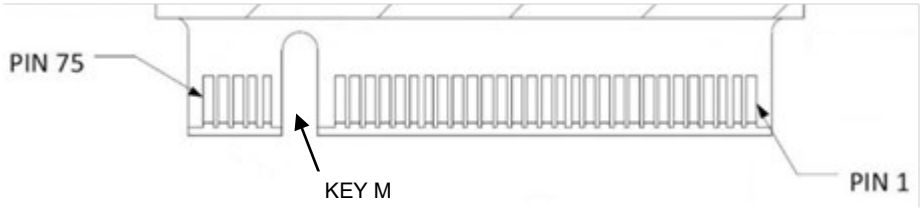

Figure 5: Signal Segment and Power Segment

3.2. Electrical Connections for M.2

A PCIe/NVMe device may be directly connected to a host or connected to a host through an adaptor card.

3.3. Device Drive

No additional device drives are required. The M.2 can be configured as a boot device.

4. Ordering Information

P/N	Capacity	Remark
AD80P3120G3DCENES	120GB	SanDisk Bics4 3D-TLC Normal Temp
AD80P3240G3DCENES	240GB	
AD80P3480G3DCENES	480GB	
AD80P3960G3DCENES	960GB	