Datasheet for DDR2

Note: ADTEC Corporation reserves the right to change products and specifications without notice.

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1. General Electrical Specifications

【Absolute Maximum DC Rating】

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage relative to V_{SS}	-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pins relative to V_{SS}	-0.5	2.3	V
T_{STG}	Storage Temperature	-55	+100	℃

【DC Operating Condition】

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Supply voltage	1.7	1.8	1.9	V	1
V_{REF}	I/O voltage reference	0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V	2,3

Note:

1. V_{DD} and V_{DDQ} are tied to each other in the module.
2. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same.
3. Peak-to-peak AC noise on V_{REF} do not exceed ±2 percent .

【DC Operating Condition for EEPROM】

Parameter	Symbol	Min.	Max.	Units	Notes
Supply Voltage	V_{DD}SPD	1.7	5.5	V	1
Input Voltage	V_{IN}	0	V_{DD}SPD	V	
"H" Input Voltage 1	V_{IH1}	0.7 x V_{DD}SPD	-	V	2
"L" Input Voltage 1	V_{IL1}	-	0.3 x V_{DD}SPD	V	2
"H" Input Voltage 2	V_{IH2}	0.8 x V_{DD}SPD	-	V	3
"L" Input Voltage 2	V_{IL2}	-	0.2 x V_{DD}SPD	V	3
"L" Output Voltage 1	V_{OL1}	-	0.4	V	4
"L" Output Voltage 2	V_{OL2}	-	0.2	V	5
Operating Current	I_{CC1}	-	2.0	mA	6
	I_{CC2}	-	0.5	mA	7
Standby Current	I_{SB}	-	2.0	μA	8
Input Leakage Current 1	I_{LI1}	-1	1	μA	9
Input Leakage Current 2	I_{LI2}	-1	15	μA	10
Output Leakage Current	I_{LO3}	-1	1	μA	11

Note:

1. Ta = -40℃ ~ +85℃
2. 2.5V≦V_{DD}SPD ≦5.5V
3. 1.7V≦V_{DD}SPD < 2.5V
4. I_{OL}=3.0mA, 2.5V≦ V_{DD}SPD ≤5.5V(SDA)
5. I_{OL}=0.7mA, 1.7V≦V_{DD}SPD < 2.5V(SDA)
6. V_{DD}SPD =5.5V,f_{SCL}=400KHz, t_{WR}=5ms, Byte Write, Page Write
7. V_{DD}SPD =5.5V,f_{SCL}=400KHz, t_{WR}=5ms, Random Read, Current Read, Sequential Read
8. V_{DD}SPD =5.5V,SDA,SCL= V_{DD}SPD, A0,A1,A2=GND,WP=GND
9. V_{IN}=0V ~ V_{DD}SPD (A0,A1,A2,SCL)
10. V_{IN}=0V ~ V_{DD}SPD (WP)
11. V_{OUT}=0V ~ V_{DD}SPD (SDA)

【Serial Interface Timing for EEPROM】

Parameter	Symbol	Fast Mode		Standard Mode		Units
		Min	Max	Min	Max	
Clock Frequency	f_{SCL}	-	400	-	100	μs
Clock High Period	t_{HIGH}	0.6	-	4.0	-	μs
Clock Low Period	t_{LOW}	1.2	-	4.7	-	μs
SDA Rise Time	t_R	-	0.3	-	1	μs
SDA Fall Time	t_F	-	0.3	-	0.3	μs
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	4.7	-	μs
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	4.0	-	μs
Input Data Setup time	$t_{SU:DAT}$	50	-	50	-	ns
Input Data Hold time	$t_{HD:DAT}$	0	-	0	-	ns
Output Data Delay time	t_{PD}	0.1	0.9	0.2	3.5	μs
Output Data Hold time	t_{DH}	0.1	-	0.2	-	μs
Stop Condition Setup Time	$t_{SU:STO}$	0.6	-	4.7	-	μs
Bus Idle	$t_{B:FREE}$	1.2	-	4.7	-	μs
Write Cycle Time	t_{WR}	-	5	-	5	ms
Noise Spike Width (SDA & SCL)	t_I	-	0.1	-	0.1	μs
WP Hold Time	$t_{HD:WP}$	0.0	-	0.0	-	ns
WP Setup Times	$t_{SU:WP}$	0.1	-	0.1	-	μs
WP High Period	$t_{HIGH:WP}$	1.0	-	1.0	-	μs

Note: Fast mode and Standard mode differ only in operation frequency. Operations performed at 100kHz are considered in "Standard-mode", while those conducted at 400kHz are in "Fast-mode".

Please note that these clock frequencies are maximum values. At lower power supply voltage it is difficult to operate at high speeds.

The EEPROM can operate at 400kHz, between 2.5V and 5.5V, and at 100kHz from 1.7V-5.5V.

【ODT DC Electrical Characteristics】

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$R_{TT1(EFF)}$	RTT effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	60	75	90	Ω	1
$R_{TT2(EFF)}$	RTT effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	120	150	180	Ω	1
$R_{TT3(EFF)}$	RTT effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1	40	50	60	Ω	1
ΔVM	Deviation of VM with respect to $V_{DD(Q)}/2$	-6	-	+6	%	2

Note:

1. $R_{TT1(EFF)}$, $R_{TT2(EFF)}$, and $R_{TT3(EFF)}$ are determined by separately applying $V_{IH}(AC)$ and $V_{IL}(DC)$ to test pin separately, and then measuring current, $I(V_{IH}(AC))$, and $I(V_{IL}(AC))$, respectively.

$$R_{TT} = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

2. Measure voltage (VM) at tested ball with no load.

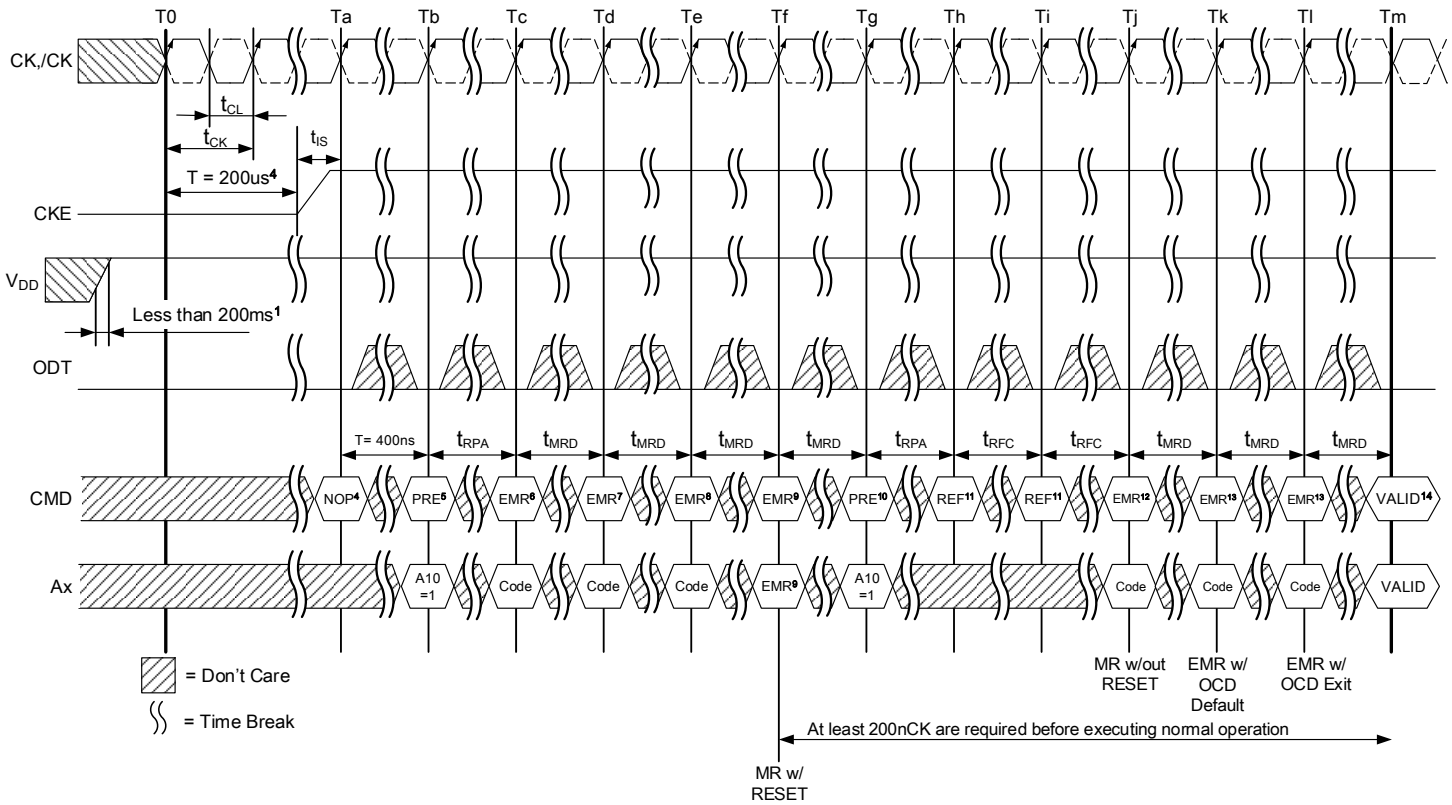
$$\Delta VM = \left(\frac{2 \times VM}{V_{DD(Q)}} - 1 \right) \times 100$$

2. Power-up and initialization Sequence

The following sequence is required for power-up and initialization, as shown in Chart1:

1. While applying power, CKE is maintained to be below 0.2 × V_{DD} during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (R_{TT} is also High-Z). The V_{DD} voltage ramp from 300mV to V_{DD} Min. must take no longer than 200ms. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in the DC operating conditions (SSTL_1.8), prevail.
2. During power-up, the following conditions may exist and must be met:
   - The voltage levels on all pins other than V_{DD} and V_{SS} must be less than or equal to V_{DD} on one side, and must be greater than or equal to V_{SS} on the other side.
   - V_{DD} voltage ramp time must be no greater than 200ms from when V_{DD} ramps from 300 mV to V_{DD} Min.
   - V_{REF} tracks V_{DD} × 0.5. V_{REF} must be within +/- 300mV with respect to V_{DD} /2 during supply ramp time.
   - V_{DD}, V_{DDQ} ≥ V_{REF} must be met at all times.
3. Start clock and maintain stable condition.
4. For the minimum of 200 us after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
5. Wait minimum of 400 ns then issue a PRECHARGE ALL command.
6. Issue an EMRS command to EMR(2). (To issue EMRS command to EMR(2), provide LOW to BA0 and BA2, HIGH to BA1.)
7. Issue an EMRS command to EMR(3). (To issue EMRS command to EMR(3), provide LOW to BA2, HIGH to BA0 and BA1.)
8. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to B A1-BA2 and A13-A15. And A9=A8=A7=LOW must be used when issuing this command.)
9. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0-BA2, and A13-A15.)
10. Issue a precharge all command.
11. Issue 2 or more auto-refresh commands.
12. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
13. At least 200 clocks after the DLL RESET, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR(1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR(1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
14. The DDR2 SDRAM is now ready for normal operation.

< Chart 1: Power-up and initialization Sequence >



Symbol	Parameter	DDR2-1066 Min	DDR2-1066 Max	DDR2-800 Min	DDR2-800 Max	DDR2-667 Min	DDR2-667 Max	DDR2-533 Min	DDR2-533 Max	DDR2-400 Min	DDR2-400 Max	Units
tCK	Clock Cycle Time	1.875	8	2.5	8	3	8	3.75	8	5	8	ns
tCL	CK Low Level Width	0.48	0.52	0.48	0.52	0.48	0.52	0.45	0.55	0.45	0.55	nCK
tIS	Address and Control Input Setup Time	Refer to the table of the Timing parameters by speed grade.										
tMRD	Mode Register Set command cycle time	2	-	2	-	2	-	2	-	2	-	nCK
tRFC 256Mb	Refresh to Activate / Refresh Interval -256Mb	75	-	75	-	75	-	75	-	75	-	ns
tRFC 512Mb	Refresh to Activate / Refresh Interval -512Mb	105	-	105	-	105	-	105	-	105	-	ns
tRFC 1Gb	Refresh to Activate / Refresh Interval -1Gb	127.5	-	127.5	-	127.5	-	127.5	-	127.5	-	ns
tRFC 2Gb	Refresh to Activate / Refresh Interval -2Gb	195	-	195	-	195	-	195	-	195	-	ns
tRFC 4Gb	Refresh to Activate / Refresh Interval -4Gb	327.5	-	327.5	-	327.5	-	327.5	-	327.5	-	ns
tRPA <1Gb	Precharge All Period	15	-	15	-	15	-	15	-	15	-	ns
tRPA ≥1Gb	Precharge All Period	20	-	18.75	-	18	-	17.5	-	15	-	ns

3. Input Electrical Characteristics and Operating Conditions

< Input DC Logic Levels >

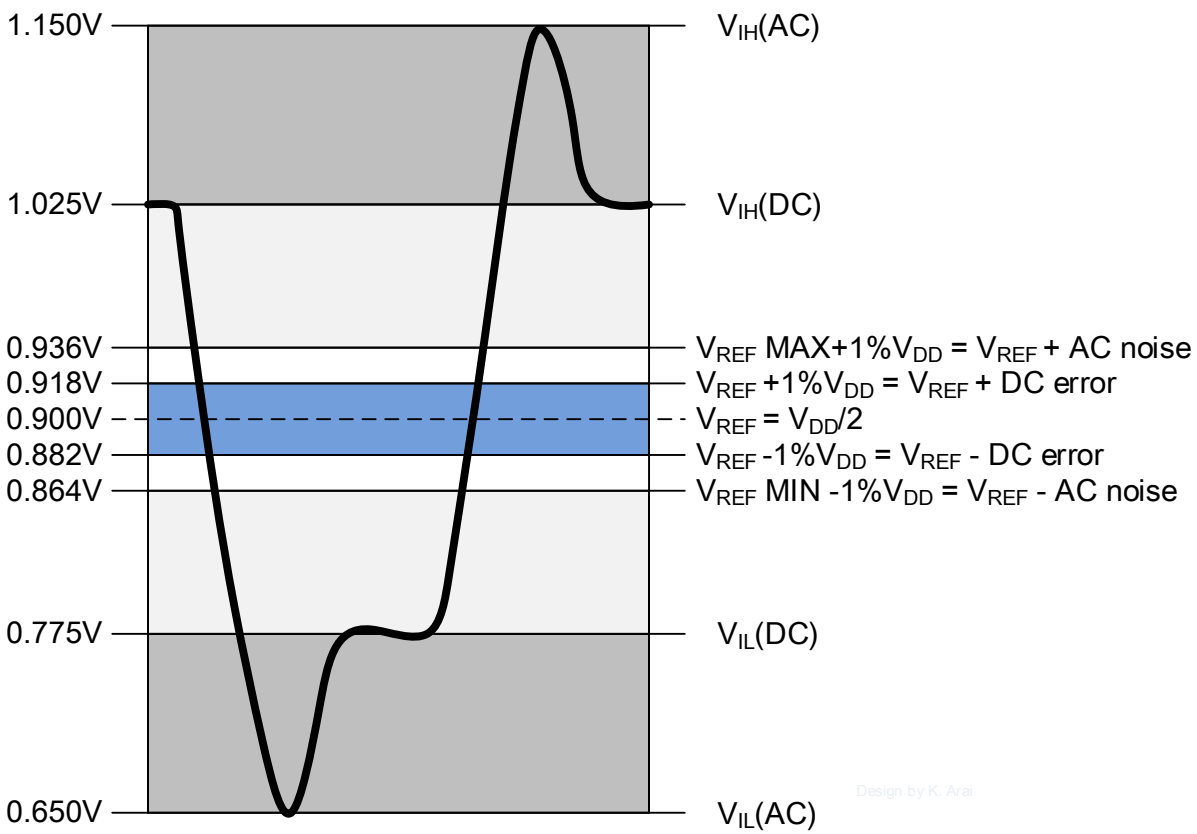
Symbol	Parameter	Min.	Max.	Units
V_{IH}(DC)	Input Logic High	V_{REF} + 0.125	V_{DD} + 0.3	V
V_{IL}(DC)	Input Logic Low	-0.3	V_{REF} - 0.125	V

< Input AC Logic Levels >

Symbol	Parameter	DDR2-400/533		DDR2-667/800/1066		Units
		Min	Max	Min	Max	
V_{IH}(AC)	Input Logic High	V_{REF} + 0.250	-	V_{REF} + 0.200	-	V
V_{IL}(AC)	Input Logic Low	-	V_{REF} - 0.250	-	V_{REF} - 0.200	V

Note: Refer to the AC overshoot/undershoot specification for the V_{IH}(AC) Max and V_{IL}(AC) Min values.

< Figure 1: DDR2 Input Signal Reference >



Note: The values in the above figure from the nominal DDR2-400/533 values (V_{DD} = V_{DDQ} = 1.8V).

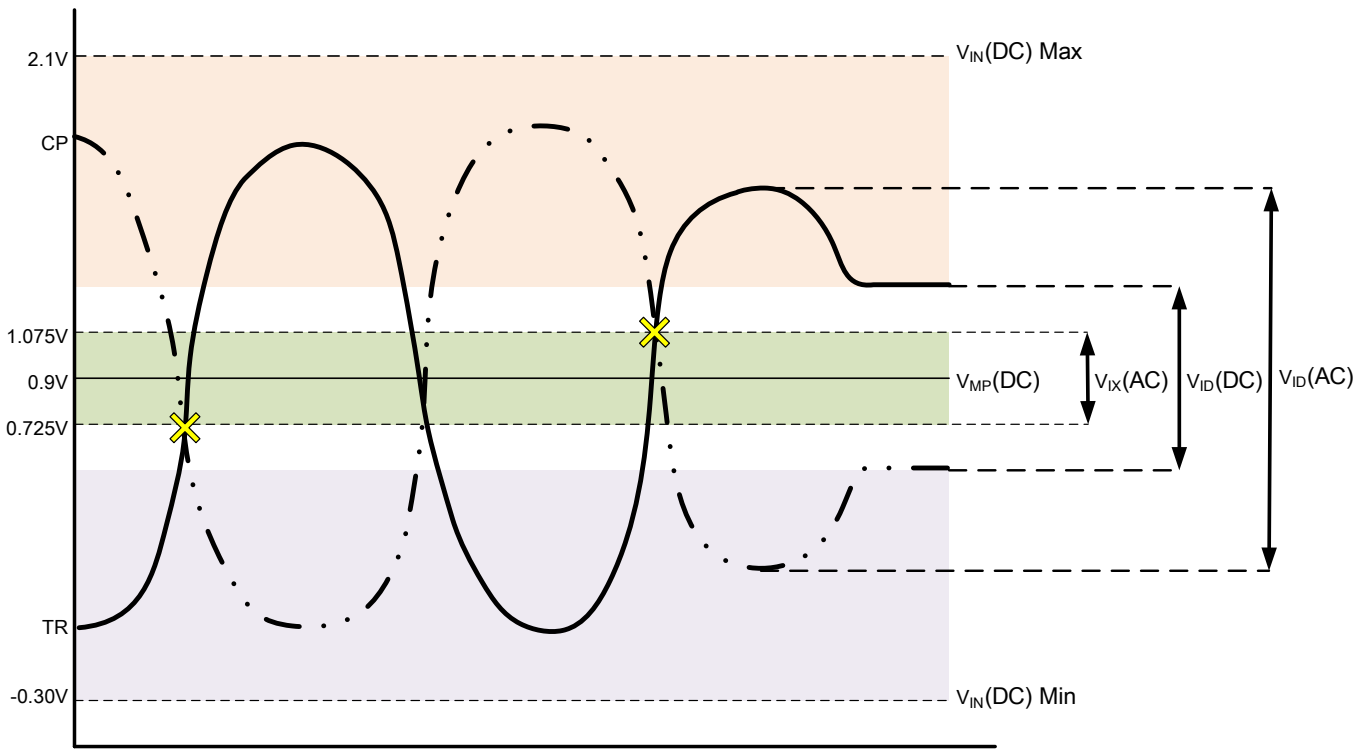
< Differential Input Logic Levels >

Symbol	Parameter	Min	Max	Units	Notes
V_{IN}(DC)	DC Input Signal Voltage	-300	V_{DD} + 300	mV	1,6
V_{ID}(DC)	DC Differential Input Voltage	250	V_{DD}	mV	2,6
V_{ID}(AC)	AC Differential Input Voltage	500	V_{DD}	mV	3,6
V_{IX}(AC)	AC Differential Cross-point Voltage	0.5 x V_{DD} - 175	0.5 x V_{DD} + 175	mV	4
V_{MP}(DC)	Input Midpoint Voltage	850	950	mV	5

Note:

1. V_{IN}(DC) specifies the allowable DC execution of each input of differential pair.
2. V_{ID}(DC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level. The minimum value is equal to V_{IH}(DC) - V_{IL}(DC).
3. V_{TR} is the true input level and V_{CP} is the complementary input level. The minimum value is equal to V_{IH}(AC) - V_{IL}(AC).
4. The typical value of V_{IX}(AC) is expected to be about 0.5 x V_{DD} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DD}. V_{IX}(AC) indicates the voltage at which differential input signals must cross.
5. V_{MP}(DC) specifies the input differential common mode voltage (V_{TR} + V_{CP})/2 where V_{TR} is the true input level and V_{CP} is the complementary input. V_{MP}(DC) is expected to be approximately 0.5 × V_{DD}.
6. V_{DD} + 300mV allowed, but the maximum value is less than 1.9V is strongly recommended.

< Figure 2: DDR2 Differential Input Signal Reference >



Note: The values in the above left side of figure when V_{DD} = V_{DDQ} = 1.8V.

4. Overshoot/Undershoot Specification

< DDR2 Over/Undershoot Specification for control and address pins[1] >

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	DDR2-1066	Units
Maximum peak amplitude allowed for overshoot area	0.50	0.50	0.50	0.50	0.50	V
Maximum peak amplitude allowed for undershoot area	0.50	0.50	0.50	0.50	0.50	V
Maximum overshoot area above V_{DD} (see Figure3)	1.33	1.00	0.80	0.66	0.66	V-ns
Maximum undershoot area below V_{SS} (see Figure4)	1.33	1.00	0.80	0.66	0.66	V-ns

Note:

1. The control and address pins are followings; An, BAn, /CS, /RAS, /CAS, /WE, CKE, & ODT.

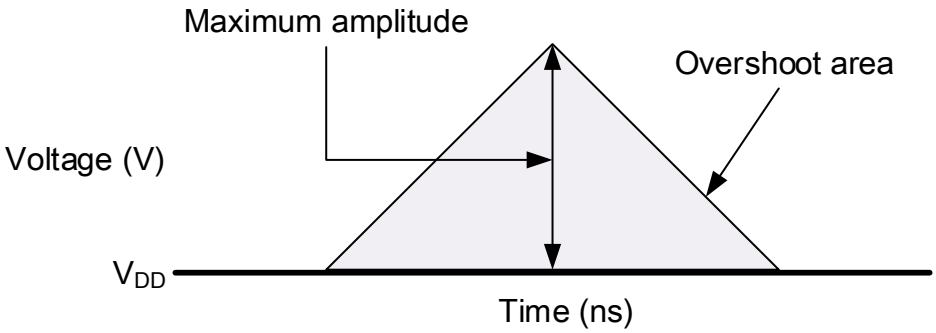
< DDR2 Over/Undershoot Specification for Clock, Data, Strobe, and Mask pins[1] >

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	DDR2-1066	Units
Maximum peak amplitude allowed for overshoot area	0.50	0.50	0.50	0.50	0.50	V
Maximum peak amplitude allowed for undershoot area	0.50	0.50	0.50	0.50	0.50	V
Maximum overshoot area above V_{DD} (see Figure3)	0.38	0.28	0.23	0.23	0.23	V-ns
Maximum undershoot area below V_{SS} (see Figure4)	0.38	0.28	0.23	0.23	0.23	V-ns

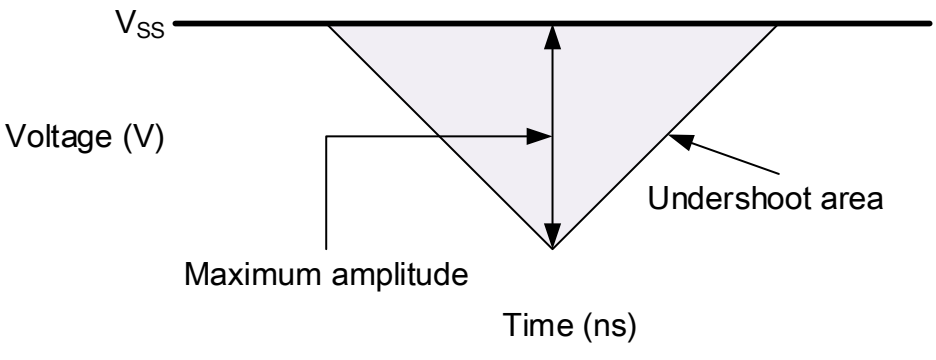
Note:

1. The control and address pins are followings; DQ, DQS, DM and those complementary signals.

< Figure 3: Overshoot >



< Figure 4: Undershoot >



5. Output Electrical Characteristics and Operating Conditions

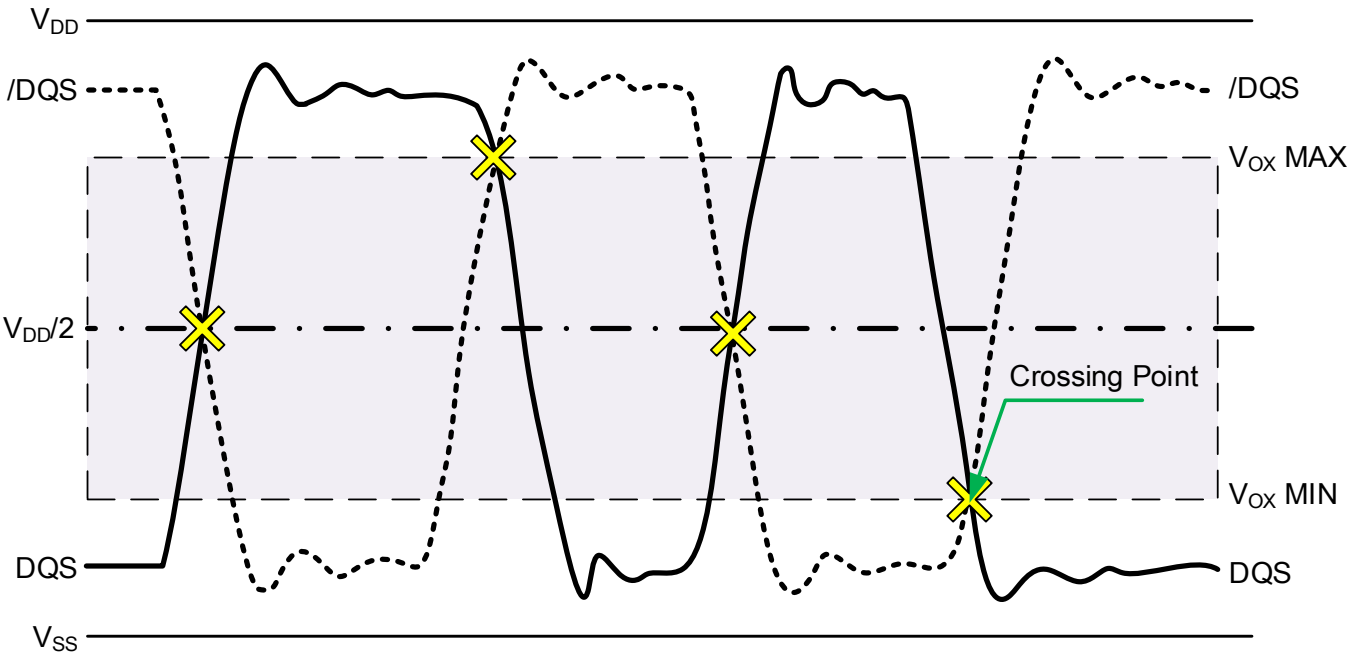
< Differential AC Output Logic Levels >

Symbol	Parameter	Min	Max	Units	Notes
V_{OX}(AC)	AC Output Crosspoint Voltage	0.5 x VDD - 0.125	0.5 x VDD + 0.125	V	1

Note:

1. The typical value of V_{OX}(AC) is expected to be about 0.5 × V_{DD} of the transmitting device and V_{OX}(AC) is expected to track variations in V_{DD}. V_{OX}(AC) indicates the voltage at which differential output signals must cross.

< Figure 5: Differential waveform >



< Output DC current drive >

Symbol	Parameter	Value	Units	Notes
I_{OH}(DC)	Output Minimum Source DC Current	-13.4	mA	1,3,4
I_{OL}(DC)	Output Minimum Sink DC Current	13.4	mA	2,3,4

Note:

1. For I_{OH}(DC); $V_{DD(Q)}$ = 1.7V, V_{OUT} = 1,420mV. (V_{OUT} - $V_{DD(Q)}$)/I_{OH} must be less than 21Ω for values of V_{OUT} between $V_{DD(Q)}$ and $V_{DD(Q)}$ - 280mV.
2. For I_{OL}(DC); $V_{DD(Q)}$ = 1.7V, V_{OUT} = 280mV. V_{OUT} /I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} MIN plus a noise margin and V_{IL} MAX minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

< DC Output Logic Levels >

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OH}(DC)	Output Logic High	V_{DD} - 0.280	V_{DD}	V	1
V_{OL}(DC)	Output Logic Low	V_{SS}	V_{SS} - 0.280	V	2

Note:

1. V_{DD} and V_{DDQ} are tied to each other in the module.
2. V_{SS} and V_{SSQ} are tied to each other in the module.

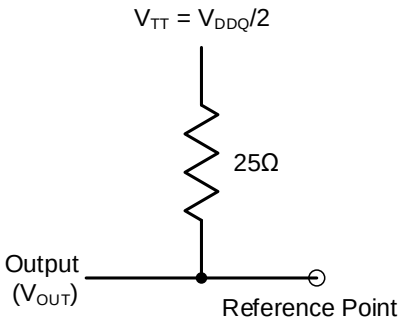
< OCD Default Characteristics>

Parameter	Min.	Typ.	Max.	Units	Notes
Output Impedance	12.6	18	23.4	Ω	1,2
Output impedance step size for OCD calibration	0	-	1.5	Ω	6
Pull-up and pull-down mismatch	0	-	4	Ω	1,2,3
Output slew rate	1.5	-	5	V/nS	1,4,5

Note:

1. Absolute specifications: 0°C ≤ T_C ≤ +85°C; $V_{DD(Q)}$ = 1.8V ±0.1V.
2. Impedance measurement conditions for output source DC current: $V_{DD(Q)}$ = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - $V_{DD(Q)}$)/I_{OH} is less than 23.4Ω for values of V_{OUT} between $V_{DD(Q)}$ and ($V_{DD(Q)}$ - 280mV). The impedance measurement condition for output sink DC current: $V_{DD(Q)}$ = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} is less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is an absolute value between pull-up and pull-down; both are measured at the same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single-ended signals. For differential signals (DQS, /DQS), output slew rate is measured between DQS - /DQS = –500mV and /DQS - DQS = 500mV. Output slew rate is guaranteed by design.
5. The absolute value of the slew rate as measured from V_{IL}(DC) MAX to V_{IH} (DC) MIN is equal to or greater than the slew rate as measured from V_{IL} (AC) MAX to V_{IH} (AC) MIN. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 Ω value(no calibration) can only be achieved if the OCD impedance is 18 +/- 0.75 Ω under nominal conditions.

< Figure 6: Reference point >

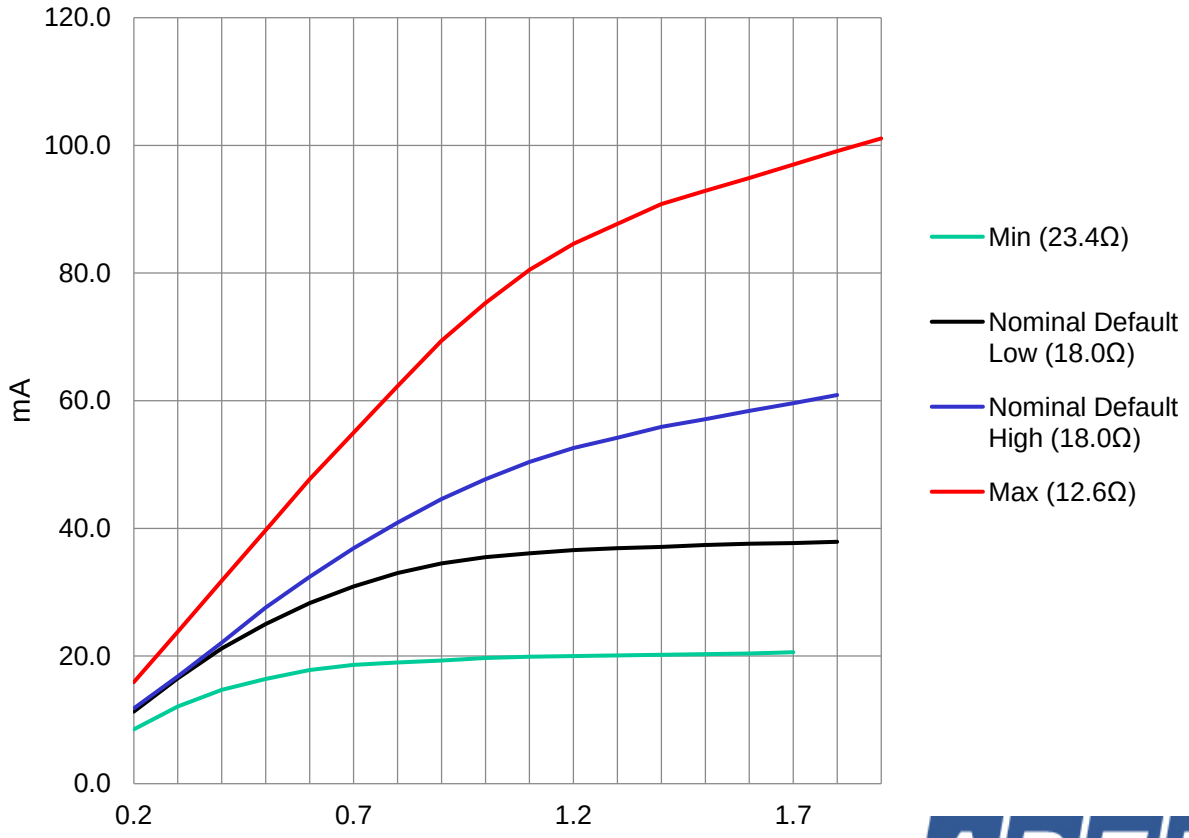


6. Default Output V-I characteristics

< Full Strength Default Pull-Down Driver Characteristics >

Voltage (V)	Min. (23.4Ω)	Nominal Default Low (18.0Ω)	Nominal Default High (18.0Ω)	Max. (12.6Ω)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

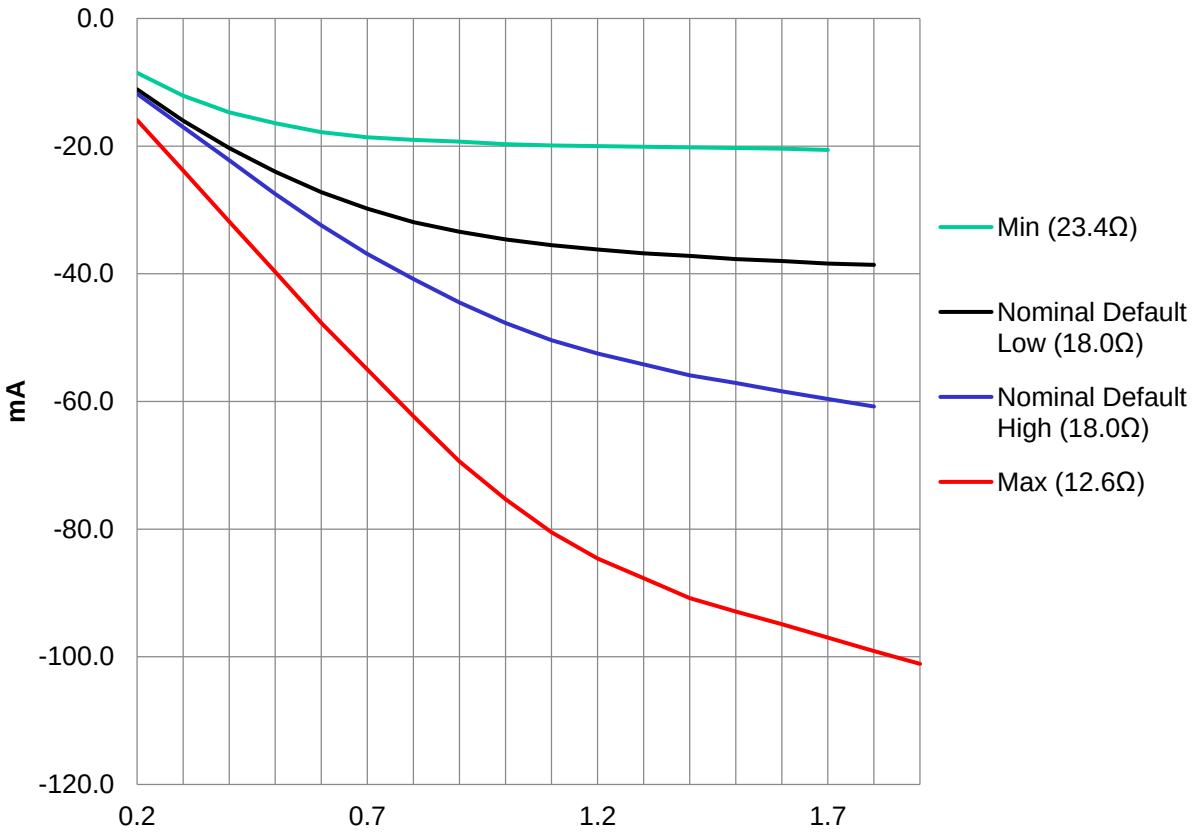
Figure 7: Full Strength Pull-Down Current



< Full Strength Default Pull-Up Driver Characteristics >

Voltage (V)	Min. (23.4Ω)	Nominal Default Low (18.0Ω)	Nominal Default High (18.0Ω)	Max. (12.6Ω)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

Figure 8: Full Strength Pull-Up Current



7. AC Operating Specifications and Conditions

< DDR2 Standard Speed Bin Table[1] >

Speed		DDR2-400	DDR2-533	DDR2-667		DDR2-800		DDR2-1066	Units	Notes
CL-*n* RCD-*n* RP		3-3-3	4-4-4	4-4-4	5-5-5	5-5-5	6-6-6	7-7-7		
Parameter	Symbol	Min	Min	Min	Min	Min	Min	Min		
ACT to READ or WRITE delay	tRCD	15	15	12	15	12.5	15	13.125	ns	3
PRECHARGE period	$^{t}_{RP}$	15	15	12	15	12.5	15	13.125	ns	2,3
ACT to ACT/REF delay	$^{t}_{RC}$	55	60	57	60	57.5	60	58.125	ns	3
ACT to PRECHARGE delay	$^{t}_{RAS}$	40	45	45	45	45	45	45	ns	3,4
Clock cycle time (CL= 3)	$^{t}_{CK(Avg)}$	5.0	5.0	5.0	5.0	5.0	5.0	5.0	ns	5
Clock cycle time (CL= 4)	$^{t}_{CK(Avg)}$	5.0	3.75	3.0	3.75	3.75	3.75	3.75	ns	5
Clock cycle time (CL= 5)	$^{t}_{CK(Avg)}$	N/A		3.0	3.0	2.5	3.0	3.0	ns	5,6
Clock cycle time (CL= 6)	$^{t}_{CK(Avg)}$	N/A					2.5	2.5	ns	5
Clock cycle time (CL= 7)	$^{t}_{CK(Avg)}$	N/A						1.875	ns	5

Note: note 1 applies to the entire table.

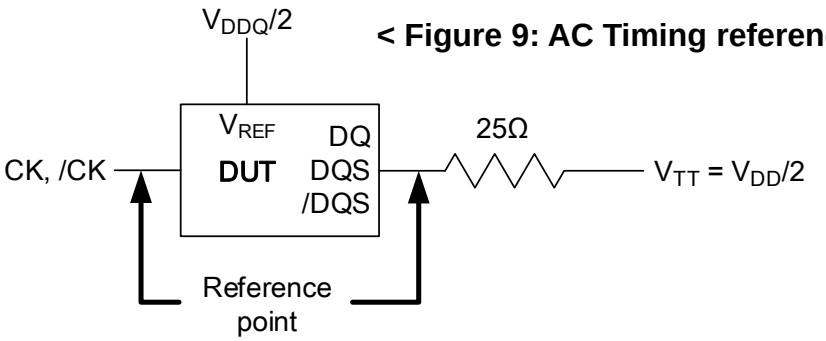
1. The speed bin table is based on JEDEC standard (JESD79-2F & 208), Support CL depends on the DRAM Grade.
2. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA timing applies when the Precharge (ALL) command is issued, regardless of the number of banks open. For 8-bank devices (≥1Gb), ^{t}RPA MIN = ^{t}RP MIN + ^{t}CK(Avg).
3. For these parameters, the DDR2 device is characterized and verified to support ^{t}PARAM(nCK) = RU(^{t}PARAM / ^{t}CK(Avg), where RU stands for round up), which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}RP(nCK) = RU(^{t}RP / tCK(Avg)), which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which ^{t}RP = 15ns, the device will support ^{t}RP(nCK) = RU(^{t}RP / ^{t}CK(Avg)) = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 – Tm) is less than 15ns due to input clock jitter.
4. All modes support ^{t}RAS MAX = 70,000ns.
5. All modes except DDR2-1066 support ^{t}CK(Avg) MAX = 8ns. Only DDR2-1066 supports up to 7.5ns.
6. DDR2-800 CL = 6 supported DRAM (SKHynix DRAM Speed Grade: S6) is not guaranteed to operate under DDR2-800 CL = 5. Its frequency must be set at 333MHz.

8.AC Parameters

< General notes, which may apply for all AC parameters >

1. The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

   The output timing reference voltage level for single ended signals is the crosspoint with V_{TT}. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. /DQS) signal.



< Figure 9: AC Timing reference point >

2. Tests for AC timing and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the operation of the device are warranted for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Slew Rate Measurement Levels
   a. Output slew rate for falling and rising edges is measured between V_{TT} - 250 mV and V_{TT} + 250 mV for single ended signals. For differential signals (e.g. DQS - /DQS) output slew rate is measured between DQS - /DQS = -500 mV and DQS - /DQS = +500mV. Output slew rate is guaranteed by design, but is not tested on each device.
   b. Input slew rate for single ended signals is measured from DC-level to AC-level: from V_{REF} - 125 mV to V_{REF} + 250 mV for rising edges and from V_{REF} + 125 mV and V_{REF} - 250 mV for falling edges.

      For differential signals (e.g. CK - CK) slew rate for rising edges is measured from CK - /CK = -250 mV to CK - /CK = +500 mV (+250mV to -500 mV for falling edges).
   c. V_{ID} is the magnitude of the difference between the input voltage on CK and the input voltage on /CK, or between DQS and /DQS for differential strobe.
4. Output slew rate is characterized under the test conditions as shown in the figure 6.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. All voltages referenced to VSS.
7. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

< Timing Parameters by Speed Grade - DDR2-400/533 (1) >

Speed			DDR2-400		DDR2-533		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max		
Clock	Clock cycle time	^{t}CK(Avg)	5.0	8.0	3.75	8.0	ns	1,2
	CK HIGH-level width	^{t}CH	Min = 0.45 Max = 0.55				nCK	
	CK LOW-level width	^{t}CL						
	Half clock period	^{t}HP	Min = lesser of ^{t}CH Min and ^{t}CL Min Max = N/A				nCK	3
Data Strobe-Out	DQS output access time from CK or /CK	^{t}DQSCK	-500	500	-450	450	ps	
	DQS Read preamble	^{t}RPRE	0.9	1.1	0.9	1.1	nCK	4
	DQS Read postamble	^{t}RPST	0.4	0.6	0.4	0.6	nCK	4
	CK/CK# to DQS Low-Z	^{t}LZ(DQS)	Min = ^{t}AC Min Max = ^{t}AC Max				ps	5,6
Data Strobe-In	DQS rising edge to CK rising edge	^{t}DQSS	-0.25	0.25	0.35	0.25	nCK	
	DQS input-high pulse width	^{t}DQSH	Min = 0.35 Max = N/A				nCK	
	DQS input-low pulse width	^{t}DQSL					nCK	
	DQS falling to CK rising: setup time	^{t}DSS	Min = 0.2 Max = N/A				nCK	
	DQS falling from CK rising: hold time	^{t}DSH					nCK	
	DQS write preamble	^{t}WPRE	0.35	-	0.35	-	nCK	
	DQS write postamble	^{t}WPST	0.4	0.6	0.4	0.6	nCK	7
	WRITE command to first DQS transition	-	Min = WL + ^{t}DQSS Min Max = WL + ^{t}DQSS Max				nCK	
Data-Out	DQ output access time from CK/CK#	^{t}AC	-600	600	-500	500	ps	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ	-	350	-	300	ps	8
	DQ hold from next DQS strobe	^{t}QHS	-	450	-	400	ps	9
	DQ–DQS hold, DQS to first DQ not valid	^{t}QH	Min = ^{t}HP x1000 - tQHS Max = N/A				ps	8
	CK/CK# to DQ, DQS High-Z	^{t}HZ	Min = N/A Max = ^{t}AC Max				ps	5,10
	CK/CK# to DQ Low-Z	^{t}LZ(DQ)	Min = 2 x ^{t}AC Min Max = ^{t}AC Max				ps	5,11
	Data valid output window	DVW	Min = ^{t}QH - ^{t}DQSQ Max = N/A				ps	8
Data-In	DQ and DM input setup time(differential strobe)	^{t}DS_Diff(base)	150	-	100	-	ps	1,12,13,15
	DQ and DM input hold time(differential strobe)	^{t}DH_Diff(base)	275	-	225	-	ps	1,12,14,15
	DQ and DM input setup time(single-ended strobe)	^{t}DS(base)	25	-	-25	-	ps	1,12,15,16
	DQ and DM input hold time(single-ended strobe)	^{t}DH(base)	25	-	-25	-	ps	1,12,15,17
	DQ and DM input pulse width	^{t}DIPW	0.35	-	0.35	-	nCK	
Command and Address	Input setup time	^{t}IS	350	-	250	-	ps	1,12,19
	Input hold time	^{t}IH	475	-	375	-	ps	1,12,19
	Input pulse width	^{t}IPW	0.6	-	0.6	-	nCK	
	Activate to Activate delay same bank	^{t}RC	55	-	60	-	ns	20,21
	Activate to Read or Write delay	^{t}RCD	15	-	15	-	ns	
	Activate to Precharge delay	^{t}RAS	40	70,000	45	70,000	ns	22,23
	Precharge period	^{t}RP	15	-	15	-	ns	24

< Timing Parameters by Speed Grade - DDR2-400/533 (2) >

Speed				DDR2-400		DDR2-533		Units	Notes
	Parameter		Symbol	Min	Max	Min	Max		
Command and Address	Precharge All period	<1Gb	^tRPA	15	-	15	-	ns	24
		≥1Gb		20	-	18.75	-		
	Activate to Activate delay different bank	x4, x8	^tRRD	7.5	-	7.5	-	ns	25
		x16		10	-	10	-		
	4-bank activate period (≥1Gb)	x4, x8	^tFAW	37.5	-	37.5	-	ns	
		x16		50	-	50	-		
	Internal Read to Precharge delay		^tRTP	7.5	-	7.5	-	ns	22,25
	/CAS to /CAS delay		^tCCD	2	-	2	-	nCK	
	Write recovery time		^tWR	15	-	15	-	ns	
	Write Auto-precharge recovery + precharge time		^tDAL	Min = ^tWR Min + ^tRP Min Max = N/A				nCK	26
	Internal Write to Read delay		^tWTR	10	-	7.5	-	ns	25
	Mode register set command cycle time		^tMRD	2	-	2	-	nCK	
Refresh	Refresh to Activate or to Refresh interval	256Mb	^tRFC	75	-	75	-	ns	27
		512Mb		105	-	105	-		
		1Gb		127.5	-	127.5	-		
		2Gb		195	-	195	-		
		4Gb		327.5	-	327.5	-		
	Average periodic refresh (0 ℃≤T_{CASE} ≤ 85℃)		^tREFI	7.8	-	7.8	-	ns	27
	Average periodic refresh (85℃ < T_{CASE} ≤ 95℃)			3.9	-	3.9	-		
	Clocks remains ON after CKE asynchronously drops LOW		^tDELAY	Min = ^tIS + ^tCK+ ^tIH Max = N/A				ns	
	Exit Self Refresh to non-Read command		^tXSNR	Min = ^tRFC Min + 10 Max = N/A				ns	
	Exit Self Refresh to Read command		^tXSRD	200	-	200	-	nCK	
Power-Down	Exit active powerdown to Read command	MR12 =0	^tXARD	2	-	2	-	nCK	
		MR12 =1		6 - AL	-	6 - AL	-		
	Exit Precharge power-down and active power-down to any non-Read command		^tXP	2	-	2	-	nCK	
	CKE Minimum HIGH/LOW pulse width		^tCKE	3	-	3	-	nCK	28
ODT/OCD	ODT to powerdown entry latency		^tANPD	3	-	3	-	nCK	
	ODT power-down exit latency		^tAXPD	8	-	8	-	nCK	
	ODT turn-on delay		^tAOND	2	2	2	2	nCK	
	ODT turn-off delay		^tAOFD	2.5	2.5	2.5	2.5	nCK	29
	ODT turn-on		^tAON	Min = ^tAC Min Max = ^tAC Max + 1000				ps	30
	ODT turn-off		^tAOF	Min = ^tAC Min Max = ^tAC Max + 600				ps	29,31
	ODT turn-on (power-down mode)		^tAONPD	Min = ^tAC Min +2000 Max = 2000 x ^tCK + ^tAC Max + 1000				ps	
	ODT turn-off (power-down mode)		^tAOFPD	Min = ^tAC Min +2000 Max = 2500 x ^tCK + ^tAC Max + 1000				ps	
	OCD drive mode output delay		^tOIT	-	12	-	12	ns	

< Timing Parameters by Speed Grade - DDR2-667/800/1066 (1) >

Speed			DDR2-667		DDR2-800		DDR2-1066		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock	Clock cycle time	^{t}CK(Avg)	3.0	8.0	2.5	8.0	1.875	7.5	ns	1,2,33
	CK HIGH-level width	^{t}CH(Avg)	Min = 0.48 Max = 0.52						^{t}CK(Avg)	33
	CK LOW-level width	^{t}CL(Avg)								
	Half clock period	^{t}HP	Min = lesser of ^{t}CH(Abs) Min and ^{t}CL(Abs) Min Max = N/A						ps	33
	Absolute ^{t}CK	^{t}CK(Abs)	Min = ^{t}CK(Avg) Min + ^{t}JITper Min Max = ^{t}CK(Avg) Max + ^{t}JITper Max						ps	33
	Absolute CK HIGH-level width	^{t}CH(Abs)	Min = ^{t}CK(Avg) Min x ^{t}CH(Avg) Min + ^{t}JITdty Min Max = ^{t}CK(Avg) Max x ^{t}CH(Avg) Max + ^{t}JITdty Max						ps	33
	Absolute CK LOW-level width	^{t}CL(Abs)	Min = ^{t}CK(Avg) Min x ^{t}CL(Avg) Min + ^{t}JITdty Min Max = ^{t}CK(Avg) Max x ^{t}CL(Avg) Max + ^{t}JITdty Max						ps	33
Data Strobe-Out	DQS output access time from CK/CK#	^{t}DQSCK	-400	400	-350	350	-325	325	ps	32,33
	DQS Read preamble	^{t}RPRE	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK(Avg)	33,34
	DQS Read postamble	^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK(Avg)	33,35
	CK/CK# to DQS Low-Z	^{t}LZ(DQS)	Min = ^{t}AC Min Max = ^{t}AC Max						^{t}CK(Avg)	5,6
Data Strobe-In	DQS rising edge to CK rising edge	^{t}DQSS	-0.25	0.25	-0.25	0.25	0.35	0.25	^{t}CK(Avg)	36
	DQS input-high pulse width	^{t}DQSH	Min = 0.35 Max = N/A						^{t}CK(Avg)	
	DQS input-low pulse width	^{t}DQSL							^{t}CK(Avg)	
	DQS falling to CK rising: setup time	^{t}DSS	Min = 0.2 Max = N/A						^{t}CK(Avg)	36
	DQS falling from CK rising: hold time	^{t}DSH							^{t}CK(Avg)	36
	DQS write preamble	^{t}WPRE	0.35	-	0.35	-	0.35	-	^{t}CK(Avg)	
	DQS write postamble	^{t}WPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK(Avg)	7
	WRITE command to first DQS transition	-	Min = WL + ^{t}DQSS Min Max = WL + ^{t}DQSS Max						^{t}CK(Avg)	
Data-Out	DQ output access time from CK or /CK	^{t}AC	-450	450	-400	400	-350	350	ps	32
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ	-	240	-	200	-	175	ps	8
	DQ hold from next DQS strobe	^{t}QHS	-	340	-	300	-	250	ps	9
	DQ–DQS hold, DQS to first DQ not valid	^{t}QH	Min = ^{t}HP - tQHS Max = N/A						ps	8
	CK/CK# to DQ, DQS High-Z	^{t}HZ	Min = N/A Max = ^{t}AC Max						ps	5,10,32
	CK/CK# to DQ Low-Z	^{t}LZ(DQ)	Min = 2 x ^{t}AC Min Max = ^{t}AC Max						ps	5,11,32
	Data valid output window	DVW	Min = ^{t}QH - ^{t}DQSQ Max = N/A						ps	8
Data-In	DQ and DM input setup time	^{t}DS(base)	100	-	50	-	0	-	ps	1,12,13,15,32
	DQ and DM input hold time	^{t}DH(base)	175	-	125	-	75	-	ps	1,12,14,15,32
	DQ and DM input pulse width	^{t}DIPW	0.35	-	0.35	-	0.35	-	^{t}CK(Avg)	
Command and Address	Input setup time	^{t}IS(base)	200	-	175	-	125	-	ps	1,12,38,39
	Input hold time	^{t}IH(base)	275	-	250	-	200	-	ps	1,12,19,39
	Input pulse width	^{t}IPW	0.6	-	0.6	-	0.6	-	^{t}CK(Avg)	
	Activate to Activate delay same bank	^{t}RC	60	-	60	-	58.125	-	ns	20,21
	Activate to Read or Write delay	^{t}RCD	15	-	15	-	13.125	-	ns	

< Timing Parameters by Speed Grade – DDR667/800/1066 (2) >

Speed				DDR2-667		DDR2-800		DDR2-1066		Units	Notes
	Parameter		Symbol	Min	Max	Min	Max	Min	Max		
Command and Address	Activate to Precharge delay		^tRAS	45	70,000	45	70,000	45	70,000	ns	22,23
	Precharge period		^tRP	15	-	15	-	13.125	-	ns	24
	Precharge All period	<1Gb	^tRPA	15	-	15	-	13.125	-	ns	24
		≥1Gb		18	-	17.5	-	15	-		
	Activate to Activate delay different bank	x4, x8	^tRRD	7.5	-	7.5	-	7.5	-	ns	25
		x16		10	-	10	-	10	-		
	4-bank activate period (≥1Gb)	x4, x8	^tFAW	37.5	-	35	-	35	-	ns	
		x16		50	-	45	-	45	-		
	Internal Read to Precharge delay		^tRTP	7.5	-	7.5	-	7.5	-	ns	22,25
	/CAS to /CAS delay		^tCCD	2	-	2	-	2	-	nCK	
	Write recovery time		^tWR	15	-	15	-	15	-	ns	
	Write Auto-precharge recovery + precharge time		^tDAL	Min = ^tWR Min + ^tRP Min Max = N/A						nCK	26
	Internal Write to Read delay		^tWTR	7.5	-	7.5	-	7.5	-	ns	25
	Mode register set command cycle time		^tMRD	2	-	2	-	2	-	nCK	
Refresh	Refresh to Activate or to Refresh interval	256Mb	^tRFC	75	-	75	-	75	-	ns	27
		512Mb		105	-	105	-	105	-		
		1Gb		127.5	-	127.5	-	127.5	-		
		2Gb		195	-	195	-	195	-		
		4Gb		327.5	-	327.5	-	327.5	-		
	Average periodic refresh (0 °C≤T_{CASE} ≤ 85°C)		^tREFI	7.8	-	7.8	-	7.8	-	ns	27
	Average periodic refresh (85°C < T_{CASE} ≤ 95°C)			3.9	-	3.9	-	3.9	-		
	Clocks remains ON after CKE asynchronously drops LOW		^tDELAY	Min = ^tIS + $^tCK(Avg)$+ ^tIH Max = N/A						ns	
	Exit Self Refresh to non-Read command		^tXSNR	Min = ^tRFC Min + 10 Max = N/A						ns	
	Exit Self Refresh to Read command		^tXSRD	200	-	200	-	200	-	nCK	
Power-Down	Exit active powerdown to Read command	MR12 =0	^tXARD	2	-	2	-	2	-	nCK	
		MR12 =1		7 - AL	-	8 - AL	-	10 - AL	-		
	Exit Precharge power-down and active power-down to any non-Read command		^tXP	2	-	2	-	3	-	nCK	
	CKE Minimum HIGH/LOW pulse width		^tCKE	3	-	3	-	3	-	nCK	28
ODT/OCD	ODT to powerdown entry latency		^tANPD	3	-	3	-	4	-	nCK	
	ODT power-down exit latency		^tAXPD	8	-	8	-	11	-	nCK	
	ODT turn-on delay		^tAOND	2	2	2	2	2	2	nCK	16
	ODT turn-off delay		^tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	nCK	41
	ODT turn-on		^tAON	Min = ^tAC Min Max = ^tAC Max + 700				Min = tAC Min Max = tAC Max + 2575		ps	30
	ODT turn-off		^tAOF	Min = ^tAC Min Max = ^tAC Max + 600						ps	31,41
	ODT turn-on (power-down mode)		^tAONPD	Min = ^tAC Min +2000 Max = 2000 x ^tCK + ^tAC Max + 1000				Min = ^tAC Min +2000 Max = 3000 x ^tCK + ^tAC Max + 1000		ps	
	ODT turn-off (power-down mode)		^tAOFPD	Min = ^tAC Min +2000 Max = 2500 x ^tCK + ^tAC Max + 1000						ps	
	OCD drive mode output delay		^tOIT	-	12	-	12	-	12	ns	

< Specific Notes for AC parameters >

1. CK and /CK input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
2. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down.
3. ^{t}CL Min, ^{t}CH Min refer to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; ^{t}CH(Avg) and ^{t}CL(Avg) must be met with or without clock jitter and with or without duty cycle jitter. ^{t}CH(Avg) and ^{t}CL(Avg) are the average of any 200 consecutive CK falling edges. ^{t}CH limits may be exceeded if the duty cycle jitter is small enough that the absolute half period limits (^{t}CH(Abs), ^{t}CL(Abs)) are not violated.
4. This parameter is not referenced to a specific voltage level but is specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
5. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
6. ^{t}LZ Min will prevail over a ^{t}DQSCK Min + ^{t}RPRE Max condition.
7. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above V_{IH}(DC) Min), then it must not transition LOW (below V_{IH}(DC)) prior to ^{t}DQSH Min.
8. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
9. ^{t}QH = ^{t}HP – ^{t}QHS, where: ^{t}HP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (^{t}CH, ^{t}CL).
10. This maximum value is derived from the referenced test load. ^{t}HZ Max will prevail over ^{t}DQSCK Max + ^{t}RPST Max condition.
11. ^{t}LZ Min will prevail over a ^{t}DQSCK Min + ^{t}RPRE Max condition.
12. Timings are guaranteed for DQs, DM, and DQS input with a differential slew rate of 2.0V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. Refer to the System Derating for other slew rate values.
13. Input waveform timing with differential data strobe enabled MR[bit10] =0, is referenced from the input signal crossing at the V_{IH}(AC) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the V_{IL}(AC) level to the differential data strobe crosspoint for a falling signal.
14. Input waveform timing with differential data strobe enabled MR[bit10] =0, is referenced from the input signal crossing at the V_{IH}(DC) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the V_{IL}(DC) level to the differential data strobe crosspoint for a falling signal.
15. If ^{t}DS or ^{t}DH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed. Regarding V_{IL}/V_{IH} overshoot/undershoot, please see AC Overshoot/Undershoot Specification in the page 8.
16. Input waveform timing with single-ended strobe enabled MR[bit10] =1, is referenced from the input signal crossing at the V_{IH}(AC) level to the single-ended data strobe crossing $V_{IH/L}$(AC) at the end of its transition for a rising signal, and from the input signal crossing at the V_{IL}(AC) level to the single-ended data strobe crossing $V_{IH/L}$(DC) at the start of its transition for a falling signal.
17. Input waveform timing with single-ended strobe enabled MR[bit10] =1, is referenced from the input signal crossing at the V_{IH}(DC) level to the single-ended data strobe crossing $V_{IH/L}$(DC) at the end of its transition for a rising signal, and from the input signal crossing at the V_{IL}(DC) level to the single-ended data strobe crossing $V_{IH/L}$(AC) at the start of its transition for a falling signal.
18. Timings are specified with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.
19. Input waveform timing is referenced from the input signal crossing at the V_{IL}(DC) level for a rising signal and V_{IH}(DC) for a falling.

20. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^{t}WR during Auto-precharge.
21. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
22. This is a minimum requirement. Minimum read to precharge timing is AL(EMR bit[5:3]) + BL/2 providing the ^{t}RTP and ^{t}RAS Min have been satisfied.
23. READs and WRITEs with Auto-precharge are allowed to be issued before ^{t}RAS Min is satisfied because ^{t}RAS lockout feature is supported in DDR2 SDRAM.
24. When a single-bank Precharge command is issued, ^{t}RP timing applies. ^{t}RPA timing applies when the Precharge (ALL) command is issued, regardless of the number of banks open. For 8-bank devices (≥1Gb), ^{t}RPA Min = ^{t}RP Min + ^{t}CK(Avg) (the "Timing Table" table lists ^{t}RP Min + ^{t}CK(Avg) Min).
25. This parameter has a two clock minimum requirement at any ^{t}CK.
26. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period. nWR refers to the ^{t}WR parameter stored in the MR9–MR11.

    Example: for DDR533 at ^{t}CK = 3.75ns with ^{t}WR programmed to 4clocks. ^{t}DAL= 4 + (15ns/3.75ns)clocks = 4 + 4clocks =8clocks.
27. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
28. ^{t}CKE Min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 × ^{t}CK + ^{t}IH.
29. For ^{t}AOFD of DDR2-400/533, the 1/2 clock of ^{t}CK in the 2.5 x ^{t}CK(Avg) assumes a ^{t}CH, input clock HIGH pulse width of 0.5 relative to ^{t}CK(Avg). ^{t}AOF Min and ^{t}AOF Max should each be derated by the same amount as the actual amount of ^{t}CH offset present at the DRAM input with respect to 0.5.

    For example, if an input clock has a worst case ^{t}CH of 0.45, the ^{t}AOF Min should be derated by subtracting 0.05 x ^{t}CK(Avg) from it, whereas if an input clock has a worst case ^{t}CH of 0.55, the ^{t}AOF Max should be derated by adding 0.05 x ^{t}CK(Avg) to it. Therefore, we have;

    ^{t}AOF Min (derated) = ^{t}AC Min - [0.5 - Min(0.5, ^{t}CH Min)] x ^{t}CK(Avg)

    ^{t}AOF Max (derated) = ^{t}AC Max + 0.6 + [Max(0.5, ^{t}CH Max) - 0.5] x ^{t}CK(Avg)

    or

    ^{t}AOF Min (derated) = Min (^{t}AC Min, ^{t}AC Min - [0.5 - ^{t}CH Min] x ^{t}CK(Avg))

    ^{t}AOF Max (derated) = 0.6 + Max (^{t}AC Max, ^{t}AC Max + [^{t}CH Max - 0.5] x ^{t}CK(Avg))

    where ^{t}CH Min and ^{t}CH Max are the minimum and maximum of ^{t}CH actually measured at the DRAM input balls.
30. ODT turn-on time ^{t}AON Min is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON Max is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
31. ODT turn-off time ^{t}AOF Min is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF Max is when the bus is in High-Z. Both are measured from ^{t}AOFD.
32. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}ERR(6~10per) of the input clock.

    For example, if the measured jitter into a DDR2-667 has ^{t}ERR(6~10per) Min = -272ps and ^{t}ERR(6~10per) Max = +293ps, then ^{t}DQSCK Min(derated) = ^{t}DQSCK Min - ^{t}ERR(6~10per) Max = -400ps - 293ps = -693ps and ^{t}DQSCK Max(derated) = ^{t}DQSCK Max - ^{t}ERR(6~10per) Min = 400ps + 272ps = +672ps.

    Similarly, ^{t}LZ(DQ) for DDR2-667 derates to ^{t}LZ(DQ) Min(derated) = -900ps - 293ps = -1193ps and ^{t}LZ(DQ) Max(derated) = 450ps + 272ps = +722ps.

33. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667, DDR2-800, and DDR2-1066 only. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameters	Symbol	DDR2-667		DDR2-800		DDR2-1066		Units
		Min	Max	Min	Max	Min	Max	
Clock period jitter	^{t}JIT(per)	-125	125	-100	100	-90	90	ps
Clock period jitter during DLL locking period	^{t}JIT(per_lck)	-100	100	-80	80	-80	80	ps
Cycle to cycle clock period jitter	^{t}JIT(cc)	-250	250	-200	200	-180	180	ps
Cycle to cycle clock period jitter during DLL locking period	^{t}JIT(cc_lck)	-200	200	-160	160	-160	160	ps
Cumulative error across 2 cycles	^{t}ERR(2per)	-175	175	-150	150	-132	132	ps
Cumulative error across 3 cycles	^{t}ERR(3per)	-225	225	-175	175	-157	157	ps
Cumulative error across 4 cycles	^{t}ERR(4per)	-250	250	-200	200	-175	175	ps
Cumulative error across 5 cycles	^{t}ERR(5per)	-250	250	-200	200	-188	188	ps
Cumulative error across n cycles, n=6...10	^{t}ERR(6~10per)	-350	350	-300	300	-250	250	ps
Cumulative error across n cycles, n=11...50	^{t}ERR(11~50per)	-450	450	-450	450	-425	425	ps
Duty cycle jitter	^{t}JIT(duty)	-125	125	-100	100	-75	75	ps

34. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JIT(per) of the input clock.

    For example, if the measured jitter into a DDR2-667 has ^{t}JIT(per) Min = -72ps and ^{t}JIT(per) Max = +93ps, then ^{t}RPRE Min(derated) = ^{t}RPRE Min + ^{t}JIT(per) Min = 0.9 x ^{t}CK(Avg) - 72ps = +2178ps and ^{t}RPRE Max(derated) = ^{t}RPRE Max + ^{t}JIT(per) Max = 1.1 x ^{t}CK(Avg) + 93ps = +2843ps.

35. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JIT(duty) of the input clock.

    For example, if the measured jitter into a DDR2-667 has ^{t}JIT(duty) Min = -72ps and ^{t}JIT(duty) Max = +93ps, then ^{t}RPST Min(derated) = ^{t}RPST Min + ^{t}JIT(duty) Min = 0.4 x ^{t}CK(Avg) - 72ps = +928ps and ^{t}RPST Max(derated) = ^{t}RPST Max + ^{t}JIT(duty) Max = 0.6 x ^{t}CK(Avg) + 93ps = +1592ps.

36. These parameters are measured from a data strobe signal crossing to its respective clock signal crossing. The spec values are not affected by the amount of clock jitter applied as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

37. These parameters are measured from a data signal transition edge to its respective data strobe signal crossing.

38. Input waveform timing is referenced from the input signal crossing at the V_{IH}(AC) level for a rising signal and V_{IL}(AC) for a falling.

39. These parameters are measured from a command/address signal transition edge to its respective clock signal crossing. The spec values are not affected by the amount of clock jitter applied, as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

40. When the device is operated with input clock jitter, this parameter needs to be derated by {-^{t}JIT(duty) Max - ^{t}ERR(6~10per) Max} and {-^{t}JIT(duty) Min - ^{t}ERR(6~10per) Min} of the actual input clock.

    For example, if the measured jitter into a DDR2-667 has tERR(6~10per) Min = -272ps, tERR(6~10per) Max = +293ps, ^{t}JIT(duty) Min = -106ps and ^{t}JIT(duty) Max = +94ps, then ^{t}AOF Min(derated) = ^{t}AOF Min + {-^{t}JIT(duty) Max - ^{t}ERR(6~10per) Max} = -450ps + {-94ps - 293ps} = -837ps and ^{t}AOF Max(derated) = ^{t}AOF Max + {-^{t}JIT(duty) Min - ^{t}ERR(6~10per) Min} = 1050ps + {106ps + 272ps} = +1428ps.

41. For ^{t}AOFD of DDR2-667/800/1066, the 1/2 clock of ^{t}CK in the 2.5 x ^{t}CK(Avg) assumes a ^{t}CH(Avg), input clock HIGH pulse width of 0.5 relative to ^{t}CK(Avg). ^{t}AOF Min and ^{t}AOF Max should each be derated by the same amount as the actual amount of ^{t}CH(Avg) offset present at the DRAM input with respect to 0.5.

    For example, if an input clock has a worst case ^{t}CH(Avg) of 0.48, the ^{t}AOF Min should be derated by subtracting 0.02 x ^{t}CK(Avg) from it, whereas if an input clock has a worst case ^{t}CH(Avg) of 0.52, the ^{t}AOF Max should be derated by adding 0.02 x ^{t}CK to it. Therefore, we have;

    ^{t}AOF Min (derated) = ^{t}AC Min - [0.5 - Min(0.5, ^{t}CH(Avg) Min)] x ^{t}CK(Avg)

    ^{t}AOF Max (derated) = ^{t}AC Max + 0.6 + [Max(0.5, ^{t}CH(Avg) Max) - 0.5] x ^{t}CK(Avg)

    or

    ^{t}AOF Min (derated) = Min (^{t}AC Min, ^{t}AC Min - [0.5 – ^{t}CH(Avg) Min] x ^{t}CK(Avg))

    ^{t}AOF Max (derated) = 0.6 + Max (^{t}AC Max, ^{t}AC Max + [^{t}CH(Avg) Max - 0.5] x ^{t}CK(Avg))

    where ^{t}CH(Avg) Min and ^{t}CH(Avg) Max are the minimum and maximum of ^{t}CH(Avg) actually measured at the DRAM input balls.

    Note that these deratings are in addition to the ^{t}AOF derating per input clock jitter. However ^{t}AC values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for ^{t}AOF are;

    ^{t}AOF Min(derated _ final) = ^{t}AOF Min(derated) + {-^{t}JIT(duty) Max - ^{t}ERR(6~10per) Max}

    ^{t}AOF Max(derated _ final) = ^{t}AOF Max(derated) + {-^{t}JIT(duty) Min - ^{t}ERR(6~10per) Min}