SDカード
TLC:32-512GB
aTLC:16-128GB

(ET1289+SanDisk Bics3/4 3D-TLC)

データシート

株式会社アドテック

Revision History

Revision	Description	Date
V1.0	New release	February 2022
V1.1	Added Ordering Information	October 2022
V1.2	Added Ordering Information	March 2023

1. Product Introduction

1.1. Overview

The Industrial SD Card is designed for demanding industrial applications.
The Industrial SD Card is compatible with SD 3.0 and provides excellent performance.
The built-in auto ECC function can detect and correct errors during data transfer.
Moreover, the Industrial SD Card supports Ultra High Speed (UHS) interface transfer mode, provides high write/read data transfer rate, high random IOPS, sudden Power Fails protection, adaptive static wear-leveling, read/program disturb management, etc.
It was designed to meet the high quality, high reliability, high performance, and versatile environmental requirements.

1.2. Product Features

- Interface: 9 pins SD standard interface
- Compliant SD Card Specification Ver. 3.0 / 4.1 / 5.1 / 6.1
- Density support:
  - 3D-TLC: 32GB~512GB
  - 3D-aTLC (Advanced TLC, single bit per cell TLC): 16GB~128GB
- Bus Speed Mode:
  - DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR12: 1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - SDR25: 1.8V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/s
- Operating at -25°C to 85°C
- Flash: 3D-TLC NAND Flash (SanDisk Bics3：3D-TLC 32GB/ Bics4：Other)
- Controller: ET1289
- Program/Erase Cycle:
  - TLC: 3,000 Cycles
  - aTLC: 30,000 Cycles
- Built-in ECC corrects up to 120bits/1 KB
- Read disturbance management (Auto-Refresh)
- Adaptive wear leveling
- Management of sudden power-fails
- SMART Function support
- aTLC (Advanced TLC, single bit per cell TLC) support, enhance the performance and product endurance.

1.3. TBW (Tera Bytes Written)

Capacity	16GB	32GB	64GB	128GB	256GB	512GB
TLC	—	57.6TB	115.2TB	230.4TB	460.8TB	921.8TB
aTLC	366.6TB	735.1TB	1469.9TB	2932.8TB	—	—

*The endurance of disk could be varying based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.
*Client workload by JESD-219A

2. SD Card Interface Description

2.1 SD Pin Assignment

Table 1: SD Bus Mode Pin Definition

Pin #	Name	Type	SD Description
1	CD/DAT3	I/O	Card Detect /Data Line [Bit3]
2	CMD	PP	Command / Response
3	VSS	S	SupplyVoltage Ground
4	VDD	S	SupplyVoltage
5	CLK	I	Clock
6	VSS	S	SupplyVoltage Ground
7	DAT0	I/O	Data Line [Bit 0]
8	DAT1	I/O	Data Line [Bit 1]
9	DAT2	I/O	Data Line [Bit2]

Notes:

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

2) The extended DAT Lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multi-media Cards.

3) After power up this line (Pin1) is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

Table 2: SPI Bus Mode Pin Definition

Pin #	Name	Type	SD Description
1	CS	I	Chip Select (neg true)
2	DI	I	Data In
3	VSS	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	SCLK	I	Clock
6	VSS	S	Supply Voltage Ground
7	DO	O	Data Out
8	RSV		Reserved
9	RSV		Reserved

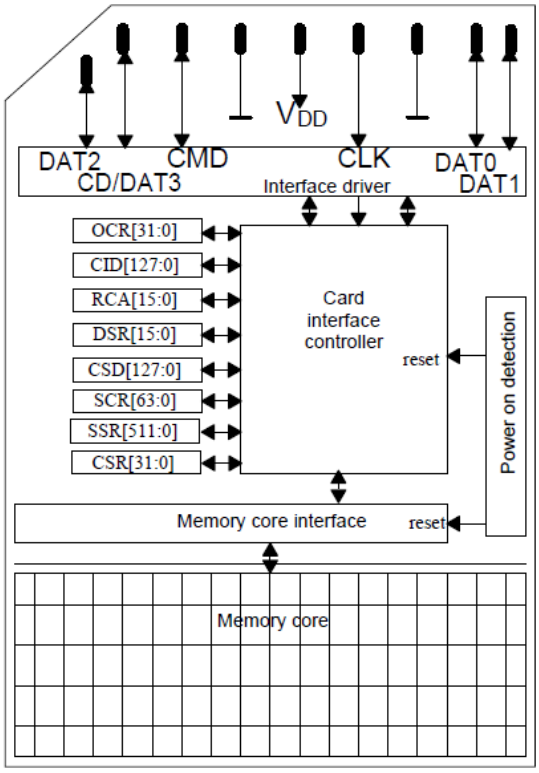

Figure 1: Functional Diagram

2.2 SD Bus Topology

The SD bus has six communication lines and three supply lines:

- CMD: Command is bi-directional signal. (Host and card drivers are operating in push pull mode.)
- DAT0-3: Data lines are bi-directional signals. (Host and card drivers are operating in push pull mode.)
- CLK: Clock is a host to cards signal. (CLK operates in push pull mode.)
- VDD: VDD is the power supply line for all cards.
- VSS: VSS is the power ground line.

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent to each card individually. However, to simplify the handling of the card stack, after initialization, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

The following figure shows the bus topology of several cards with one host in SD Bus mode.

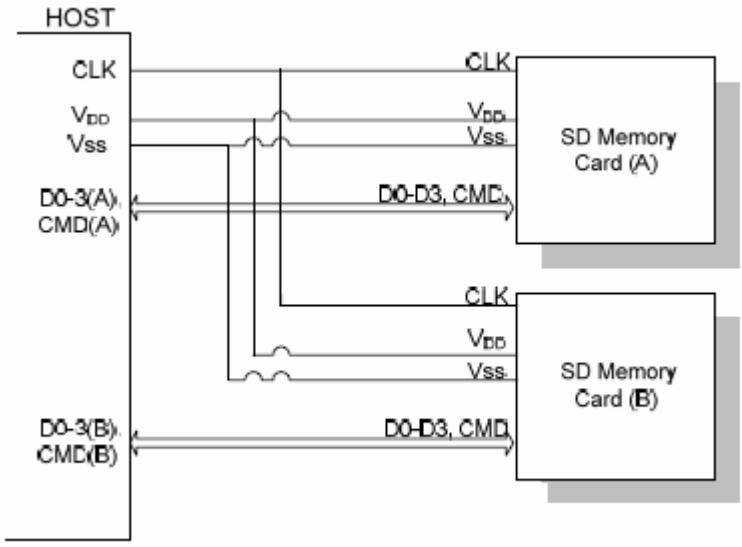

Figure 2: Memory Card System Bus Topology

2.3 SPI Bus Topology

The memory Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device, the SD Memory Card SPI channel consists of the following 4 signals:

- CS: Host to card Chip Select signal.
- CLK: Host to card clock signal.
- Data In: Host to card data signal.
- Data Out: Card to host data signal.

Another SPI common characteristic, which is implemented in the Memory Card as well, is byte transfers. All data tokens are multiples of 8bit bytes and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands, a card (slave) is selected by asserting (active low) the CS signal. The CS signal shall be continuously active for the duration of the SPI transaction (command, response, and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT2 are not used, DAT3 is the CS signal) of the SD bus.

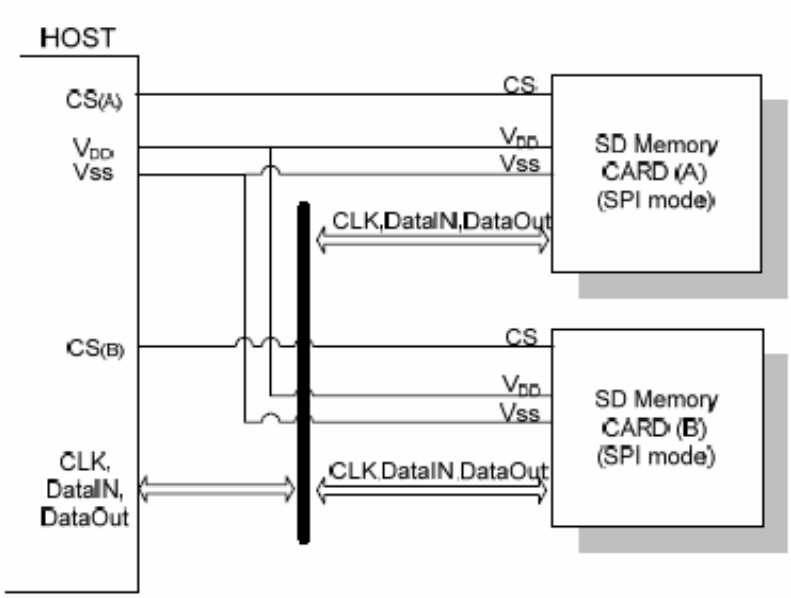

Figure 3: SPI mode SD Memory Card Bus System

3. Specifications

3.1 Performance

Max. Data Transfer Rate

- Read: 90MB/s; Write: 70MB/s

3.2 NAND Flash Memory

Industrial SD Card uses Triple Level Cell (TLC) NAND Flash memory, which is non- volatility, high reliability and highspeed memory storage.

3.3 Power Requirement

3.3.1. DC Input Voltage

- 2.7V to 3.6V

3.4 Temperature Range

- -25°C to +85°C

3.5 Humidity

Relative Humidity: 5-95%, non-condensing

3.6 Waterproof

Waterproof level: IEC 60529 IPX8.

Test Condition	Referred standard
Depth of water 1.5m for 30 mins.	IEC 60529 IPX8

3.7 ESD Ability

Test Condition	Referred standard
● Contact discharge: ± 2KV, ± 4KV	SD Spec. Appendix D.1
● Air discharge: ± 4KV, ± 8KV, ± 15KV	SD Spec. Appendix D.2

3.8 Dust Proof

Dust proof level: IEC 60529 IP6X.

Test Condition	Referred standard
Depression of 2 KPa, Talcum powder 2kg/m³, 8 hrs.	IEC 60529 IP6X

4. Electrical Specifications

4.1 General DC Character

Table 3: General DC Character

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines	—	-0.3	3.6	V	
All input leakage current	—	-10	10	μA	
All output leakage current	—	-10	10	μA	
Supply voltage for low voltage range	V_{DDL}	—	—	V	
Supply voltage for high voltage range	V_{DDH}	2.7	3.6	V	
Supply voltage differential	—	-0.5	0.5	V	

4.2 Bus Signal Line Loading

Table 4: Bus Signal Line Loading

Parameter	Symbol	Min	Max	Unit	Remark
Pull up resistance for SD command line	R_{CMD}	4.7	100	KΩ	
Pull up resistance for SD data line	R_{DAT}	10	100	KΩ	
Total Bus capacitance for each signal line	C_L	—	30	pF	
Signal line inductance	—	—	16	pF	
Pull-up resistance inside card (pin 1)	R_{DAT3}	10	150	KΩ	

4.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

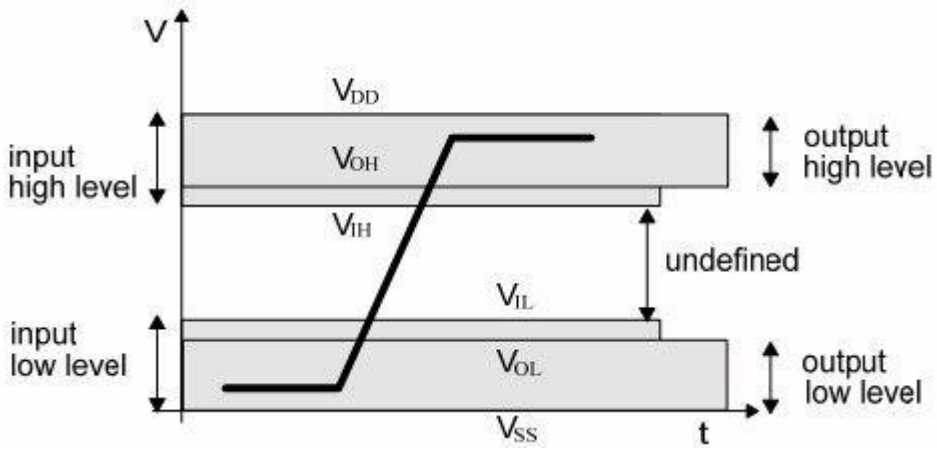

Figure 4: Bus Signal Levels

Table 5: Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Remark
Output High Voltage	V_{OH}	2.4	—	V	V_{DD} = 3.3V
Output Low Voltage	V_{OL}	—	0.4	V	V_{DD} = 3.3V
Input High Voltage	V_{IH}	2.0	3.6	V	V_{DD} = 3.3V
Input Low Voltage	V_{IL}	-0.3	0.8	V	V_{DD} = 3.3V
Output High Voltage	V_{OH}	1.4	—	V	V_{DD} = 1.8V
Output Low Voltage	V_{OL}	—	0.45	V	V_{DD} = 1.8V
Input High Voltage	V_{IH}	1.26	2.1	V	V_{DD} = 1.8V
Input Low Voltage	V_{IL}	-0.3	0.58	V	V_{DD} = 1.8V

4.4 Bus Timing (Default Speed Mode)

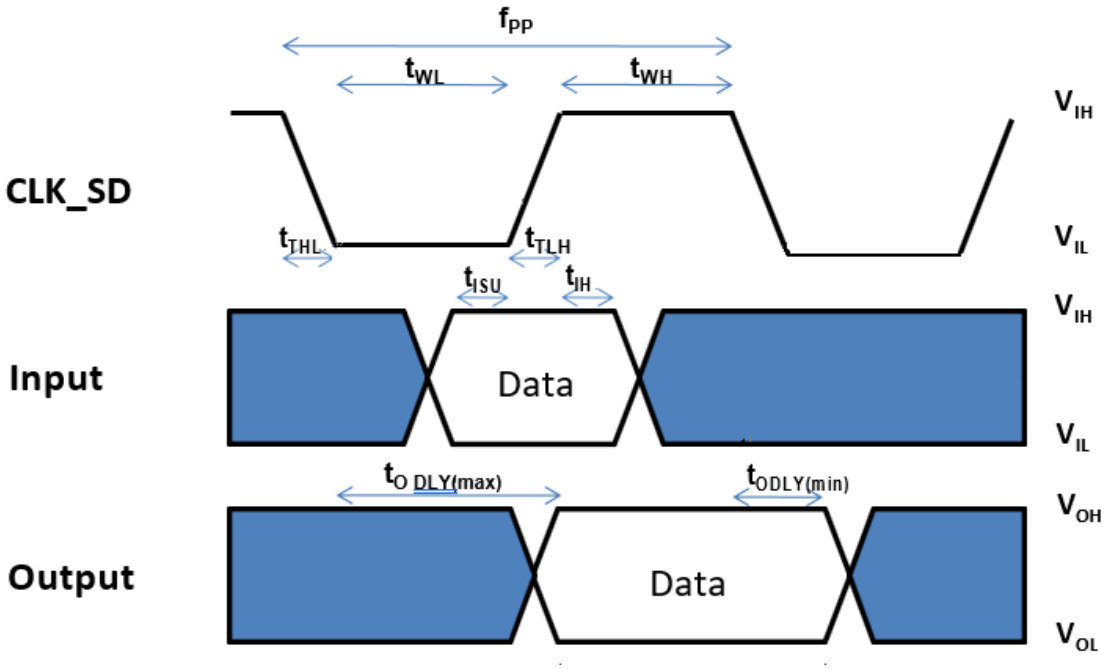

Figure 5: Timing diagram data input/output referenced to clock (Default Speed Mode)

Table 6: Bus Timing - Parameters Values (Default Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{pp}	—	25	MHz	$C_L \leqq$ 10pF (1 card)
Clock frequency Identification mode	f_{OD}	—	400	KHz	$C_L \leqq$ 10pF (1 card)
Clock low time / Clock high time	t_{WL}/t_{WH}	10	—	ns	$C_L \leqq$ 10pF (1 card)
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	—	10	ns	$C_L \leqq$ 10pF (1 card)
Input CMD_SD/DATA_SD, referenced to CLK_SD					
Input set-up time	t_{ISU}	5	—	ns	$C_L \leqq$ 10pF (1 card)
Input hold time	t_{IH}	5	—	ns	$C_L \leqq$ 10pF (1 card)
Output CMD_SD/DATA_SD, referenced to CLK_SD					
Output Delay time during Data Transfer Mode	t_{ODLY}	—	14	ns	$C_L \leqq$ 40pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	—	50	ns	$C_L \leqq$ 40pF (1 card)

(1) All timing values are measured relative to 50% of voltage level.
(2) Rise and fall times are measured from 10% - 90% of voltage level.

4.5 Bus Timing (High-Speed Mode)

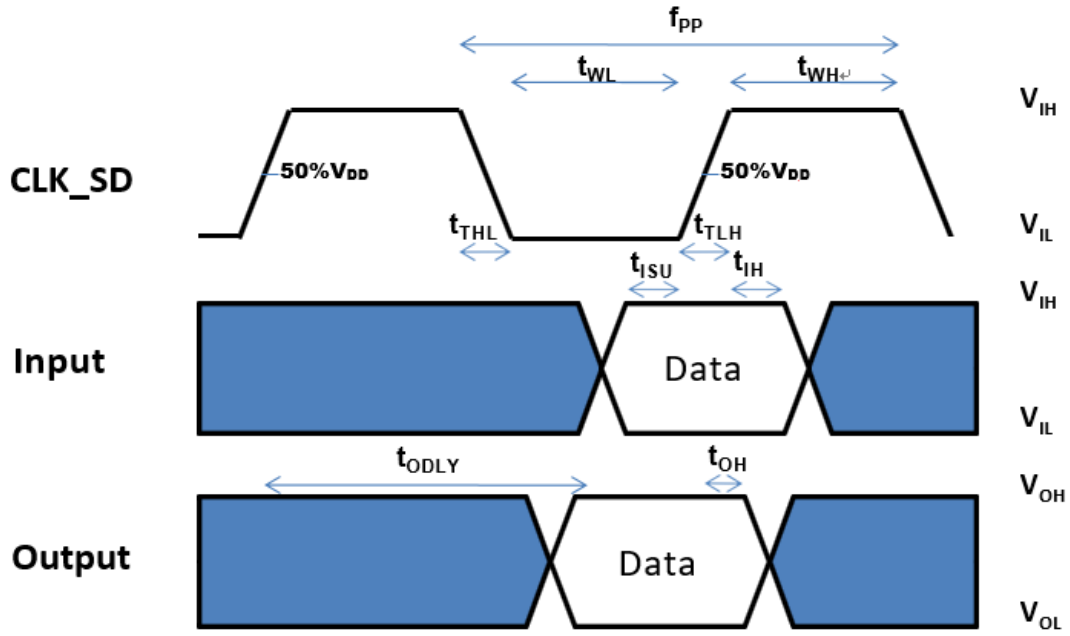

Figure 6: Timing diagram data input/output referenced to clock (High-Speed Mode)

Table 7: Bus Timing - Parameters Values (High-Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	$C_L \leqq$ 10pF (1 card)
Clock low time / Clock high time	t_{WL}/t_{WH}	7	—	ns	$C_L \leqq$ 10pF (1 card)
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	—	3	ns	$C_L \leqq$ 10pF (1 card)
Input CMD_SD/DATA_SD, referenced to CLK_SD					
Input set-up time	t_{ISU}	6	—	ns	$C_L \leqq$ 25pF (1 card)
Input hold time	t_{IH}	2	—	ns	$C_L \leqq$ 25pF (1 card)
Output CMD_SD/DATA_SD, referenced to CLK_SD					
Output Delay time during Data Transfer Mode	t_{ODLY}	—	14	ns	$C_L \leqq$ 40pF (1 card)
Output hold time	t_{OH}	2.5	—	ns	$C_L \geqq$ 15pF (1 card)
Total System capacitance for each line	C_L	—	40	pF	

(1) All timing values are measured relative to 50% of voltage level.
(2) Rise and fall times are measured from 10% - 90% of voltage level.

Table 8: Bus Timing - Parameters Values (SDR104/SDR50/SDR25/SDR12)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{PP}	0	208	MHz	C_L = 10pF
Clock cycle time	t_{CLK}	4.8	—	ns	C_L = 10pF
Clock duty cycle		30	70	%	
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	—	0.2*t_{CLK}	ns	C_L = 10pF
Input CMD_SD/DATA_SD, referenced to CLK_SD					
Input set-up time for SDR104	t_{ISU}	1.4	—	ns	C_L = 10pF
Input set-up time for SDR50	t_{ISU}	3	—	ns	C_L = 10pF
Input hold time	t_{IH}	0.8	—	ns	C_L = 5pF
Output CMD_SD/DATA_SD, referenced to CLK_SD					
Output Delay time for SDR50	t_{ODLY}	—	7.5	ns	C_L = 30pF, using driver Type B
Output Delay time for SDR25 and sdr12	t_{ODLY}	—	14	ns	C_L = 40pF, using driver Type B
Output hold time	t_{OH}	1.5	—	ns	C_L = 15pF
Total System capacitance for each line	C_L	—	40	pF	

4.6 Bus Timing (DDR Mode)

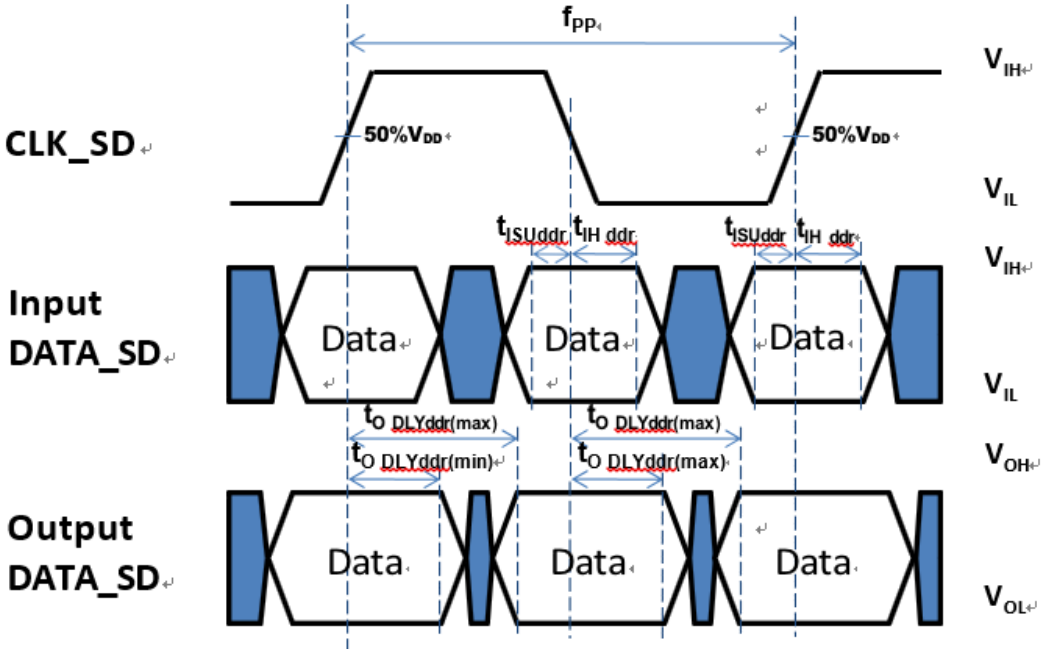

Figure 7: Timing diagram data input/output referenced to clock (DDR Mode)

Table 9 : Bus Timing - Parameters Values(DDR)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock duty cycle		45	55	%	
Input CMD_SD, referenced to CLK_SD					
Input set-up time	t_{ISU}	3	—	ns	$C_L \leqq$ 10pF (1 card)
Input hold time	t_{IH}	0.8	—	ns	$C_L \leqq$ 10pF (1 card)
Output CMD_SD, referenced to CLK_SD					
Output Delay time during data transfer mode	t_{ODLY}	—	13.7	ns	$C_L \leqq$ 30pF (1 card)
Output hold time	t_{OH}	1.5	—	ns	$C_L \geqq$ 15pF (1 card)
Input DATA_SD, referenced to CLK_SD					
Input set-up time	t_{ISUddr}	3	—	ns	$C_L \leqq$ 10pF (1 card)
Input hold time	t_{IHddr}	0.8	—	ns	$C_L \leqq$ 10pF (1 card)
Output DATA_SD, referenced to CLK_SD					
Output Delay time during data transfer mode	$t_{ODLYddr}$	—	7	ns	$C_L \leqq$ 25pF (1 card)
Output hold time	t_{OHddr}	1.5	—	ns	$C_L \geqq$ 15pF (1 card)

5. Mechanical Dimensions

The mechanical dimensions of industrial SD card were basically followed the mechanical form factor definitions on SD-Memory card specifications which constructed by SD card association.

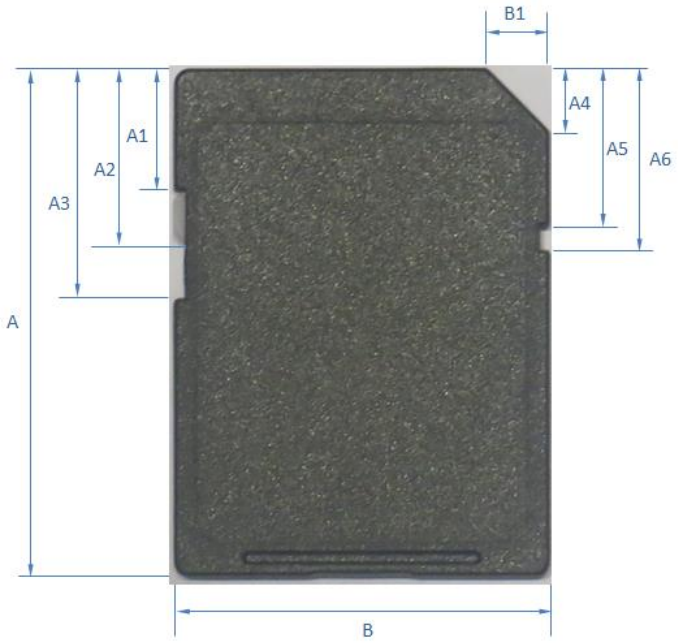

Figure 13: Top View

Criteria of SD — Unit: mm

Dimensions	Min	TYP	Max	Note
A	31.90	32.00	32.10	
B	23.90	24.00	24.10	
A1	7.65	7.80	7.95	
A2	10.70	10.85	11.00	
A3	14.35	14.50	14.65	
A4	3.85	4.00	4.15	
A5	9.85	10.00	10.15	
A6	11.35	11.50	11.65	
B1	3.85	4.00	4.15	
C1	7.00			
C2			4.00	
C3	2.20	2.30	2.40	
C4	0.20			
C5			1.60	
C6	5.00			
C7	5.95			
D1	1.40			
D2	1.10			
D3	0.90			
E	0.60	0.75	0.90	
P	2.35	2.50	2.65	
P1	5.475	5.625	5.775	
P2	7.90	8.05	8.20	
P3	9.60	9.75	9.90	
T	1.95	2.10	2.25	
T1	1.25	1.40	1.55	
T2	1.30	1.40	1.60	
W1	0.55	0.70	0.85	
W2	0.45	0.60	0.75	
R	0.15	0.30	0.45	

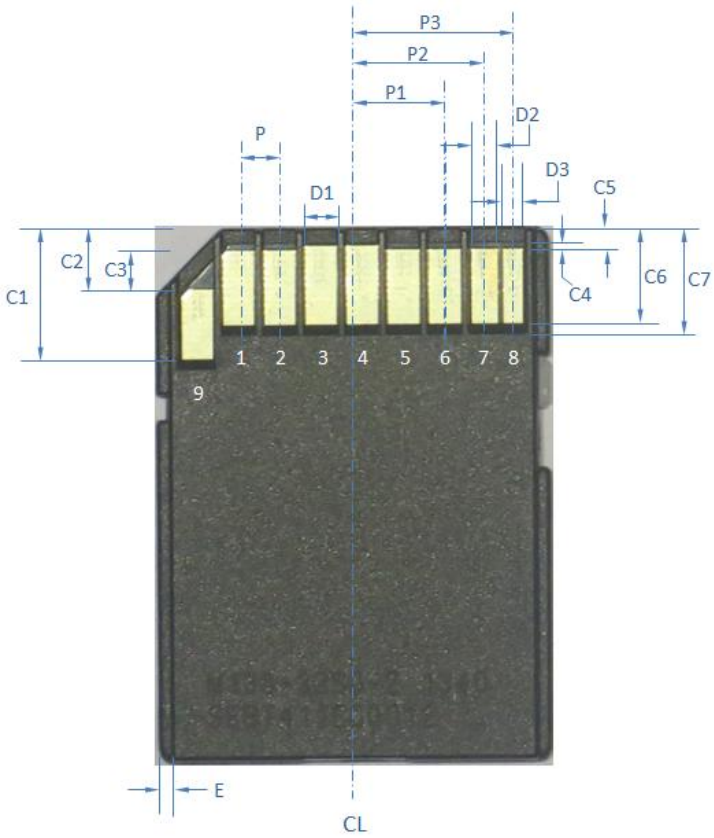

Figure 14: Bottom View

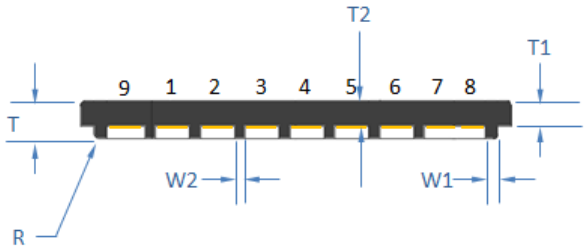

Figure 15: Side View

6. Ordering Information

Flash Type	Part Number	Capacity	Note
TLC	ADS1U1032G3DAEDES	32GB	Bics3
	ADS1U1064G3DCEDES	64GB	
	ADS1U1128G3DCEDES	128GB	
	ADS1U1256G3DCEDES	256GB	
	ADS1U1512G3DCEDES	512GB	
aTLC	ADS1U1016GPDCEDES	16GB	
	ADS1U1032GPDCEDES	32GB	
	ADS1U1064GPDCEDES	64GB	
	ADS1U1128GPDCEDES	128GB	